

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Eliyahou Harari et al.		
Title:	Flash EEPROM System		
Application No.:	10/000,155	Filing Date:	November 30, 2001
Examiner:	Mai, Son Luu	Group Art Unit:	2818
Docket No.:	SNDK.A06US8	Conf. No.:	8242

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APPELLANT'S BRIEF UNDER 37 C.F.R. 41.37
ON APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

In response to the Notice of Non-Compliant Appeal Brief filed in this application on April 24, 2007, Applicants submit this Appeal Brief. A three-month extension of the reply period is requested, thereby extending the reply period to August 24, 2007. The Commissioner is authorized to deduct any amounts required for this Appeal Brief and to credit any amounts overpaid to Deposit Account No. 040258.

TABLE OF CONTENTS

	<u>Page</u>
I. Real Party in Interest	3
II. Related Appeals and Interferences	3
III. Status of the Claims	4
IV. Status of Amendments	5
V. Summary of the Claimed Subject Matter	5
VI. Grounds of Rejection to Reviewed on Appeal	8
VII. Argument	8
VIII. Conclusion	10
IX. Appendix A: Text of Pending Application Claims	12
X. Evidence Appendix	21
XI. Related Proceedings Appendix	22

I. REAL PARTY IN INTEREST

The real party in interest is SanDisk Corporation, a corporation of the state of Delaware, the assignee of all right, title and interest in the present patent application from the inventors, Eliyahou Harari, Robert D. Norman, and Sanjay Mehrotra.

II. RELATED APPEALS AND INTERFERENCES

Several applications that share disclosure with the present application, all similarly claiming priority from, and limited to the matter disclosed in, US patent application number 07/337,566, have been involved in an appeal, interference, or judicial proceeding. Although they may not have a direct bearing on the present appeal, the following list is provided here through an abundance of caution:

US patent application number 09/103,056 has been involved in Patent Interference No. 104,760. The decision from this Interference is included in the Related Proceedings Appendix.

US patent application number 09/056,398 has been involved in an Appeal. The decision from this Appeal is included in the Related Proceedings Appendix.

A Notice of Appeal and Appeal brief were filed in US patent application number 10/417,954, but the appeal did not go forward and the examiner reopened prosecution. Consequently, there is no decision and the inclusion of one is *not applicable*.

An appeal is currently pending in US patent application number 09/114,504. Consequently, there is as yet no decision and the inclusion of one is *not applicable*.

An appeal is currently pending in US patent application number 09/143,233.. Consequently, there is as yet no decision and the inclusion of one is *not applicable*.

US patent number 5,418,752 has been involved in a U.S. International Trade Commission action, Investigation No. 337-TA-382. The decision from this action is included in the Related Proceedings Appendix.

US patent number 5,991,517 has been involved in a U.S. International Trade Commission action, Investigation No. 337-TA-560. The decision from this action is included in the Related Proceedings Appendix.

US patent number 5,602,987 has been involved in litigation, *SanDisk Corporation v. Lexar Media, Inc.*, United States District Court for Northern California, San Francisco Division, Case No. C98-0111 CRB (PJH). This case was settled. Consequently, there is no decision and the inclusion of one is *not applicable*.

US patent number 5,602,987 is involved in pending litigation. The decision from an appeal in this case, *SanDisk Corporation v. Memorex Products, Inc.*, 415 F.3d 1278, 75USPQ 2D1475 (Fed. Cir. 2005), is included in the Related Proceedings Appendix.

US patent number 5,719,808 is involved in pending litigation, *STMicroelectronics, Inc. v. SanDisk Corporation v. STMicroelectronics, Inc.*, United States District Court for the Eastern District of Texas, Sherman Division, Case Action No. 4:05CV45. Consequently, there is as yet no decision and the inclusion of one is *not applicable*.

III. STATUS OF THE CLAIMS

The subject application is a continuation of patent application serial no. 09/280,385, filed March 3, 1999, now abandoned, which is a continuation of patent application serial no. 08/771,708, filed December 20, 1996, now patent no. 5,991,517, which is a continuation of patent application serial no. 08/174,768, filed December 29, 1993, now patent no. 5,602,987, which is a continuation of patent application serial no. 07/963,838, filed October 20, 1992, now patent no. 5,297,148, which in turn is a division of patent application serial no. 07/337,566, filed April 13, 1989, abandoned. The original parent application claims 1-62 were cancelled in a Preliminary Amendment filed concurrently with the subject application on November 30, 2001. This Preliminary Amendment also added claims 63-97, which were, respectively, copies of claims 1-3, 5, 7-9, 14-16, 18, 20-21, 25-27, 31-35, 37, 39-46, 48 and 50-53 of U.S. patent no. 6,141,267 - Kiriata *et al.* granted October 31, 2000.

In the first Office Action on the merits (January 31, 2003), claims 63-97 were rejected under 35 U.S.C.112, first paragraph, for the written description requirement due to a number of elements. A Response (mailed April 25, 2003) to the first Office Action argued that the 35 U.S.C. 112, first paragraph, rejections were not well founded and that the written description requirement was met. A second Office Action (July 30, 2003) rejecting claims 63-97 was based on new grounds, but again under 35 U.S.C.112, first paragraph, for failing to comply with the

written description for "a memory array comprising a plurality of groups of ... address cells, said cells in each of said groups of ... address cells ... storing ... addresses". A Response (mailed September 24, 2003) to the second Office Action argued that the 35 U.S.C. 112, first paragraph, rejection was not well founded and that the written description requirement was met. Three more Office Actions on the same basis followed, with a Response in reply to each arguing that the 35 U.S.C. 112, first paragraph, rejection was not well founded and that the written description requirement was met. In an attempt to try and clarify the bases of these rejections, the Response to the fifth Office Action (and the fourth on the same basis) added claims 98-103, which are similar to, and correspond to, the previously pending independent claims, but having some what differing language. The most recent Office Action (mailed May 19, 2005) extended to previous basis of rejection to these newly added claims as well.

Claims 63-103 stand rejected under 35 U.S.C. §112, first paragraph, as the Applicants allegedly failed to comply with the written description for "a memory array comprising a plurality of groups of ... address cells, said cells in each of said groups of ... address cells ... storing ... addresses".

Claims 1-62 have been cancelled.

IV. STATUS OF AMENDMENTS

On November 17, 2005, a Notice of Appeal from the Examiner's decision rejecting claims 63-103 was filed. No Amendments have been filed since the May 19, 2005, mailing date of the Office Action from which this Appeal is being taken.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

As background, this section gives a summary of the present invention. Since the claims stand rejected under the written description requirement of 35 U.S.C. §112, first paragraph, some of this material is presented in more detail below in section VII in order to demonstrate that adequate description is supplied in the specification of the subject application.

The claimed subject matter is a memory system and method of operating it for managing defects in a memory array. The memory array includes two sets of groups of memory cells, the first of these groups for the storing of data and the other of these groups for storing addresses.

When one or more of these groups of cells are accessed, to read the data content for example, the memory determines whether an inputted address matches one of these groups. If such an address match condition is detected, the corresponding data from the accessed group is output.

The pending independent claims are claims 68, 71, and 74. In claim 68, the memory is presented as:

68. A memory comprising:
a plurality of word lines;
a plurality of bit lines; and
a plurality of memory cells, wherein each of said memory cells corresponds to a selected one of said plurality of word lines and a selected one of said plurality of bit lines;
wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells being provided for storing data and said second group of memory cells being provided for storing attribute data of said first group of memory cells, wherein said attribute data includes a number of rewriting of said first group of memory cells.

Claim 71 differs from 68 in that it is for “a plurality of cell blocks” and that it specifies the size of the “first group of memory cells” rather than specifying that the “attribute data” includes the “number of rewriting”. (Consequently, note that ground of rejection based on the “number of rewriting” does not apply to claim 71.) Claim 71 is:

71. A memory including a plurality of memory cell blocks, each of said plurality of memory cell blocks comprising:
a plurality of word lines;
a plurality of bit lines; and
a plurality of memory cells, each of said plurality of memory cells being connected between one of said word lines and one of said bit lines;
wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, wherein said first group of memory cells are provided for storing data and said second group of memory cells are provided for storing attribute data of said first group of memory cells, and wherein said first group of memory cells are memory cells storing 512 bytes.

Claim 74 differs from 68 in that it specifies “a plurality of cell blocks”:

74. A memory comprising:
a plurality of memory cell blocks further comprising;
a plurality of word lines;
a plurality of bit lines; and
a plurality of memory cells, wherein each of said plurality of memory cells corresponds to a selected one of said word lines and a selected one of said bit lines; and wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells provided for storing data and said second group of memory cells provided for storing attribute data of said first group of memory cells, and wherein said attribute data includes a rewriting number of said first group of memory cells.

In the application, the basic structure of the memory system is discussed in the “EEprom System” section, which begins at the top of page 6. Some of detail on the structure of the memory chips, such as shown in Figures 1 and 2 of the present application, is discussed in more detail in US patent application serial number 204,175, now patent number 5,095,344 (“’344”), which is incorporated by reference at numerous places in the present application: Figures 15a and 15b of ’344 show a memory with each cell corresponding to a selected one of the rows (word lines) and a selected one of the columns (bit lines). The structure is discussed more in section VIII of the ’344 patent beginning at column 32, line 57.

The present patent application primarily describes this subject matter in the “Defect Mapping” section that begins on line 12 of page 14 of the specification. The various access, detection, and output circuit are shown for a read process in Figure 6, which is primarily described beginning on page 17, line 26. Many of the independent claims use means plus function language, such as in claim 98, for example. The “means for accessing ...” can be taken to include elements 503, 511, and 513 of Figure 6, described between page 17, line 16, to page 18, line 28. The “means for detecting an address match condition ...” can be taken to include elements 509 and 521 as described on page 19, lines 17-22. The “means for outputting data ...” can be taken to include elements 515, 517, 519, and 525 of Figure 6, described between page 18, line 18, to page 20, line 2.

The groups of memory cells storing data and addresses, whose alleged lack of description is the sole issue in this appeal, are shown in Figure 5. This figure shows an exemplary partition of memory sectors according to the present application. Figure 5 is primarily described beginning at line 23 of page 16. According to this sector partition, the sectors include a first group of memory cells, 403 “DATA”, that store data and a second group of memory cells, 409 “DEFECT MAP”, that store the addresses of defective cells and backup cells.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Board is asked to review the correctness of the rejections under 35 U.S.C. §112, first paragraph. Specifically, claims 63-103 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. The Office Action alleges that “the specification fails to describe groups of address cells for storing address[es] in a memory array.” This is the basis for rejecting all of the independent claims and is the sole issue in this appeal. All of the claims can be taken to form a single group, with independent claim 98 suitable for deciding whether the group of claims is patentable.

VII. ARGUMENT

The most recent Office Action, from which this Appeal originates, rejects all of the pending claims under 35 U.S.C. §112, first paragraph, for failing to comply with the written description requirement. All of these claims are rejected on the same ground, namely a lack of written description for “a memory array comprising a plurality of groups of ... address cells, said cells in each of said groups of ... address cells ... storing ... addresses”, where this or a similar limitation is found in all of the independent claims. Consequently, all of the claims are argued together and, when reference to a specific claim is required, claim 98 is believed suitable for this purpose.

Claim 98 begins:

98. A defect management engine comprising:
 a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses;

where support for support for “a plurality of groups of first cells ..., said cells in each of said groups of first cells ... storing data” is not questioned. It is on “a plurality of groups of ... second cells, said cells in each of said groups of ... second cells ... storing ... addresses” that the Office Action bases its rejection.

Figure 5, as described primarily between line 23 of page 16 and line 25 of page 17, shows a typical memory sector 401 whose cells are organized into a data portion 403 and a “spare portion” 405. (The “cells ... storing data” correspond to DATA 403 and can also be taken to include ALTERNATE DEFECTS DATA 407.) The cells of the “spare portion” are further

organized to include a “defect map area” 409. As stated at page 17, lines 6-8: “The **addresses** of the defective cell **are stored** as defect pointers **in the defect map 409.**” Thus, as the added emphasis shows, there is clear disclosure of a group of cells storing addresses. As there are a plurality of such sectors (see, e.g., Figure 2 or Figure 3A), there are a corresponding plurality such groups. Consequently, it is believed that the present application clearly provides suitable written description of “a plurality of groups of ... cells ... storing ... addresses” and that the rejection under 35 U.S.C. §112, first paragraph, is not well founded.

In its Response to Arguments section, the Office Action from which this Appeal originates states (page 3, last paragraph):

At the bottom of page 11 and on page 12 [of the last Amendment], the Applicants again argued that the present application provides support for “address cells ... storing ... addresses”. On the contrary, the specification on page 17, lines 6-8, only describes the addresses of the defective cell and the backup cell stored as defect pointers in the defect map 409.

The emphasis and ellipses are in the original. From the last sentence in this quote, the Office Action admits that the specification “describes the addresses ... stored” in the memory cells of “the defect map”; but, rather, the Office Action seems to be basing its rejection on this support stating that these addresses are stored in the form of “defect pointers”; that is, the Office Action is rejecting the claims *not* based on a lack of support *for the claim element itself*, but is instead basing it on some further requirement *not found in the claim itself*. (As for the “defect” part of “defect pointers”, it should be noted that the preamble explicitly states that the claim is for a “defect management engine”; thus, the substance of the rejection appears to be based on an objection to the *form* in which the addresses being stored (“pointers”), a limitation not found in the claims.)

Based on these comments, the Office Action seems to be requiring that present application provide not just support for the claims as written, but for a specific embodiment—or, perhaps more accurately, seems to require support for ruling out a particular embodiment. This is improper. The correct question is whether the present specification is enabling for the claims *as written*. The claims contain ***no such limiting language*** (such as “wherein said addresses are not stored as pointers” or other such limiting language) that would restrict that would restrict them in this way. As noted in 37 CFR 41.200(b), “[a] claim shall be given it broadest reasonable construction. ...”. Similarly, as noted in the M.P.E.P. §2111, claims must be given their broadest

reasonable interpretation; in contrast, the Office Action appears to be reading limitations into the claim that are not there and then improperly issuing a rejection on this basis. As noted above, support for the disputed claim element *as written* is explicitly given at page 17, lines 6-8 of the specification: "The addresses ... are stored ... defect map".

(As noted above in Section III above, the currently pending claims in the present application are either copied from, or correspond to claims found in U.S. patent 6,141,267. Although not explicitly stated in the Office Actions, it may be that the Office Action is requiring that present application provide not just support for the claims as written, but for a specific embodiment of U.S. patent 6,141,267. (This mistake was explicitly made in the first Office Action for the present application, see the Office Action mailed January 31, 2003, last paragraph beginning on page 2.) This is again improper and the correct question is whether the present specification is enabling for the claim *as written*.)

Consequently, for any of these reasons, it is respectfully submitted that the rejection of claims 63-103 under the first paragraph of 35 U.S.C. §112 is not well founded and should be withdrawn. As described above, the specification is believed to more than satisfy the written description require for "a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses".

VIII. CONCLUSION

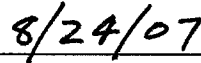
It is Applicants' position, as indicated above, that the assertions of the Office Action are incorrect. The subject matter of the claims is provided with an adequate written description by

the subject application. Accordingly, the rejection of the application should be reversed and the present patent application passed to issue.

Respectfully submitted,



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Appendix A

CLAIMS PENDING IN APPLICATION SERIAL NO. 10/000,155

Claims 1-62 are cancelled.

63. A defect management engine comprising:

a memory array comprising a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses;

means for accessing at least one of said plurality of groups of data cells and address cells;

means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and

means for outputting data from said accessed group of data cells when said address match condition is detected.

64. The defect management engine as recited in claim 63, further comprising at least one main memory wherein said data cells are redundancy data cells for replacing defective ones of said data cells in said at least one main memory, and said address cells are redundancy address cells for storing addresses of defective ones of data cells in said at least one main memory.

65. The defect management engine as recited in claim 63 further comprising means for overriding said accessed group of data cells respectively with new data, when said address match condition is detected

66. The defect management engine as recited in claim 63, wherein said data cells and said address cells are of a same cell type.

67. The defect management engine as recited in claim 63, wherein addresses stored in said address cells are non-volatile.

68. The defect management engine as recited in claim 63 further comprising means for programming addresses stored in said address cells.

69. The defect management engine recited in claim 64, wherein said redundancy data cells are of a same cell type as said data cells in said at least one main memory

70. The defect management engine as recited in claim 68, wherein said means for programming is enabled by a command generated by a controller means.

71. The defect management engine as recited in claim 68, wherein said means for programming replicates said addresses into said address cells by sequentially activating each of said address cells.

72. The defect management engine as recited in claim 68, wherein said means for programming replicates said addresses into said address cells by simultaneously activating at least two of said address cells.

73. The defect management engine as recited in claim 64 further comprising means for enabling a single-bit and a multi-bit redundancy replacement within said at least one main memory.

74. The defect management engine as recited in claim 73, wherein said multi-bit size redundancies replace multiple defective ones of said data cells within said at least one main memory with one group of said plurality of groups of redundancy data cells

75. The defect management engine as recited in claim 73 further comprising means for enabling a variable bit size redundancy replacement in said at least one main memory.

76. The defect management engine as recited in claim 64, wherein said data cells are redundancy data cells for replacing defective ones of said data cells present in at least one domain within said at least one main memory, and said address cells are redundancy address cells for addressing defective ones of said data cells within said at least one domain.

77. The defect management engine as recited in claim 76, wherein said plurality of groups of redundancy data cells and redundancy address cells is assigned to said at least one domain.

78. The defect management engine as recited in claim 76, wherein said at least one domain within said at least one main memory is supported by at least one of said plurality of groups of redundancy data cells and redundancy address cells.

79. The defect management engine as recited in claim 63, wherein said means for accessing at least one of said plurality of groups includes wordline drivers.

80. The defect management engine as recited in claim 79, wherein said means for accessing at least one of said plurality of groups further includes sense amplifiers.

81. The defect management engine as recited in claim 79, wherein said wordline driver enables means for assigning to said plurality of groups of data cells and address cells respective redundancy ones of said redundancy data cells and redundancy address cells to repair a plurality of faults in at least one of said domains.

82. A defect management engine coupled to at least one main memory comprising:
a memory array comprising a plurality of groups of redundancy data cells and redundancy address cells, said cells in each of said groups of redundancy data cells and redundancy address cells respectively storing redundancy data and redundancy addresses;
means for accessing at least one of said plurality of groups of redundancy data cells and redundancy address cells;
means for detecting a redundancy address match condition for each of said accessed groups, wherein the redundancy address of said accessed group matches one of a plurality of inputted addresses; and

means for outputting redundancy data from said accessed group of redundancy data cells and redundancy address cells when said redundancy address match condition is detected.

83. The defect management engine as recited in claim 82 further comprising means for overriding said accessed group of redundancy data cells with new data when said redundancy address match condition is detected.

84. The defect management engine as recited in claim 82, wherein said redundancy data cells and said redundancy address cells are of a same cell type

85. A defect management system comprising a plurality of memory chips, and at least one defect management engine chip coupled to each of said memory chips, said at least one defect management engine chip comprising:

a memory array comprising a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses;

means for accessing at least one of said plurality of groups of data cells and address cells;

means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and

means for outputting data from said accessed group of data cells when said address match condition is detected.

86. The defect management system as recited in claim 85 further comprising a non-volatile random access memory chip coupled to each of said memory chips.

87. A defect management system comprising a plurality of chips, each of said chips comprising at least one memory, and at least one defect management engine coupled to said at least one memory, said at least one defect management engine comprising: a memory array comprising a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses; means for accessing at least one of said plurality of groups of data cells and address cells; means for detecting an

address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and means for outputting data from said accessed group of data cells when said address match condition is detected.

88. The defect management system as recited in claim 87 further comprising at least one non-volatile random access memory coupled to said at least one memory and to said at least one defect management engine.

89. A defect management system comprising a plurality of chips, each of said chips comprising at least one memory, at least one non-volatile random access memory coupled to said at least one memory, and at least one defect management engine coupled to said at least one memory, said at least one defect management engine comprising: a memory array comprising a plurality of groups of data cells and address cells said cells, in each of said groups of data cells and address cells respectively storing data and addresses; means for accessing at least one of said plurality of groups of data cells and address cells; means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and means for outputting data from said accessed group of data cells when said address match condition is detected.

90. The defect management system as recited in claim 89 further comprising at least one defect management engine chip coupled to each of said chips comprising said at least one memory and to said at least one non-volatile random access memory.

91. A method of managing defects comprising the steps of:

configuring a memory array in a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses;

accessing at least one of said plurality of groups of data cells and address cells;

detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches one of a plurality of inputted addresses; and

outputting data from said accessed group of data cells and address cells when said address match condition is detected.

92. The method of managing defects as recited in claim 91 further comprising the step of overriding with new data said accessed group of data cells when said address match condition is detected.

93. The method of managing defects as recited in claim 91, wherein said data cells and said address cells are of a same cell type.

94. The method of managing defects as recited in claim 91, wherein the addresses stored in said address cells are non-volatile.

95. The method of managing defects as recited in claim 91 further comprising means for programming said addresses stored in at least one of said address cells.

96. A method of managing defects comprising the steps of:

- configuring a memory array into a plurality of groups of redundancy data cells and redundancy address cells, said cells respectively storing redundancy data and redundancy addresses;
- accessing at least one of said plurality of groups of redundancy data cells and redundancy address cells;
- detecting a redundancy address match condition for each of said accessed groups, wherein the redundancy address of said accessed group of redundancy address cells matches one of a plurality of inputted addresses; and
- outputting redundancy data from said accessed group of redundancy data cells and redundancy address cells when said redundancy address match condition is detected.

97. The defect management engine as recited in claim 96 further comprising the step of overriding with new data said accessed group of redundancy data cells when said redundancy address match condition is detected.

98. A defect management engine comprising:
a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses;
means for accessing at least one of said plurality of groups of first cells and second cells;
means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and
means for outputting data from said accessed group of first cells when said address match condition is detected.

99. A defect management engine coupled to at least one main memory comprising:
a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing backup data and backup addresses;
means for accessing at least one of said plurality of groups of first cells and second cells;
means for detecting a backup address match condition for each of said accessed groups, wherein the backup address of said accessed group matches one of a plurality of inputted addresses; and
means for outputting backup data from said accessed group of first cells and second cells when said backup address match condition is detected.

100. A defect management system comprising a plurality of memory chips, and at least one defect management engine chip coupled to each of said memory chips, said at least one defect management engine chip comprising:
a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses;
means for accessing at least one of said plurality of groups of first cells and second cells;

means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and

means for outputting data from said accessed group of first cells when said address match condition is detected.

101. A defect management system comprising a plurality of chips, each of said chips comprising at least one memory, and at least one defect management engine coupled to said at least one memory, said at least one defect management engine comprising: a memory array comprising a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses; means for accessing at least one of said plurality of groups of first cells and second cells; means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and means for outputting data from said accessed group of first cells when said address match condition is detected.

102. A method of managing defects comprising the steps of:

configuring a memory array in a plurality of groups of first cells and second cells, said cells in each of said groups of first cells and second cells respectively storing data and addresses;

accessing at least one of said plurality of groups of first cells and second cells;

detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches one of a plurality of inputted addresses; and

outputting data from said accessed group of first cells and second cells when said address match condition is detected.

103. A method of managing defects comprising the steps of:

configuring a memory array into a plurality of groups of first cells and second cells, said cells respectively storing backup data and backup addresses;

accessing at least one of said plurality of groups of first cells and second cells;

detecting a backup address match condition for each of said accessed groups,
wherein the backup address of said accessed group of second cells matches one of a plurality of
inputted addresses; and

outputting backup data from said accessed group of first cells and second cells
when said backup address match condition is detected.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

DECISION ON PRELIMINARY MOTIONS

PATENT INTERFERENCE NO. 104,760

**DECISION ON YAMAGAMI SECOND REQUEST FOR RECONSIDERATION AND
FINAL JUDGMENT, PATENT INTERFERENCE NO. 104,760**

DECISION ON APPEAL, APPEAL NO. 2001-1272

U.S. INTERNATIONAL TRADE COMMISSION, INVESTIGATION NO. 337-TA-382

U.S. INTERNATIONAL TRADE COMMISSION, INVESTIGATION NO. 337-TA-560

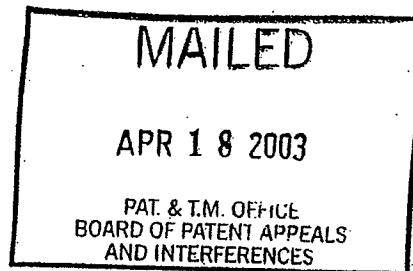
**DECISION ON APPEAL, *SANDISK CORPORATION V. MEMOREX PRODUCTS, INC.*,
415 F.3D 1278, 75USPQ 2D1475 (FED. CIR. 2005)**

DECISION ON PRELIMINARY MOTIONS
PATENT INTERFERENCE NO. 104,760

The opinion in support of the decision being entered today
is not binding precedent of the Board.

Paper No. 91

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Senior Party.
(S.N. 09/103,056)

Patent Interference No. 104,760

Before: LEE, CRAWFORD, and MEDLEY, Administrative Patent Judges.

CRAWFORD, Administrative Patent Judge.

DECISION ON PRELIMINARY MOTIONS

This interference, which was declared on October 30, 2001, with a single count, is before a motions panel for a decision on preliminary motions.

The following preliminary motions are before us:

Yamagami's preliminary motion number 1 pursuant to 37 CFR § 1.633(a) for judgment on the grounds that Harari's claims 63 and 64 are unpatentable (Paper No. 22). Opposition (Paper No. 47). Reply (Paper No. 59).

Yamagami's preliminary motion number 2 pursuant to 37 CFR § 1.633(c)(4) to designate claim 14 as not corresponding to the count (Paper No. 23). Opposition (Paper No. 48). Reply (Paper No. 60).

Yamagami's preliminary motion number 3 pursuant to 37 CFR § 1.633(f) for benefit of earlier filed applications (Paper No. 24). Opposition (Paper No. 49). Reply (Paper No. 61).

Yamagami's preliminary motion number 4 pursuant to 37 CFR § 1.633(g) attacking the benefit accorded Harari in the notice declaring this interference (Paper No. 25). Opposition (Paper No. 50). Reply (Paper No. 62).

Yamagami's preliminary motion number 5 pursuant to 37 CFR § 1.633(c)(3) to redefine the interfering subject matter by designating claims 65 and 66 as corresponding to the count (Paper No. 26). Opposition (Paper No. 51). Reply (Paper No. 63).

Interference No. 104,760

Yamagami's contingent preliminary motion number 6 pursuant to 37 CFR § 1.633(a) for a judgment that claims 65 and 66 are unpatentable (Paper No. 27). Opposition (Paper No. 52). Reply (Paper No. 64).

Yamagami's contingent preliminary motion number 7 pursuant to 37 CFR § 1.633(g) attacking the benefit accorded Harari in the notice declaring the interference as to newly added claims 65 and 66 (Paper No. 28). Opposition (Paper No. 53). Reply (Paper No. 65).

Yamagami's contingent preliminary motion number 8 pursuant to 37 CFR § 1.633(a) to hold claims 63 and 64 of the Harari application unpatentable (Paper No. 29). Opposition (Paper No. 54). Reply (Paper No. 66).

Harari's preliminary motion number 1 pursuant to 37 CFR § 1.633(a) for judgment that claims 9 and 14 of the Yamagami patent are not patentable (Paper No. 32). Opposition (Paper No. 41). Reply (Paper No. 55).

Harari's preliminary motion number 2 pursuant to 37 CFR § 1.633(c)(2) to redefine the interfering subject matter by adding claims 67 and 68 (Paper No. 38). Opposition (Paper No. 42). Reply (Paper No. 56).

Harari's contingent preliminary motion number 3 pursuant to 37 CFR § 1.633(c)(1) and (i) to substitute a count (Paper No. 39). Opposition (Paper No. 43). Reply (Paper No. 57).

Harari's contingent preliminary motion number 4 pursuant to 37 CFR § 1.633(f) to be accorded the benefit of the filing date of earlier applications for the added claims 67 and 68 (Paper No. 40). Opposition (Paper No. 44). Reply (Paper No. 58).

Findings of Fact

1. The count of this interference is claim 63 of the involved Harari application ("Harari application") or claim 9 of the involved Yamagami patent ("Yamagami patent"). The two claims read the same as follows:

A storage device employing a flash memory, wherein a storage area of said storage device is divided into a plurality of physical sectors identified by physical addresses, said storage device includes:

logical address conversion means which receives a logical address of data in a data writing operation and converts said logical address into a physical address, and

a memory controller for receiving said physical address resulting from the conversion by the conversion means, and writing said data into a respective physical sector;

wherein said logical address conversion means converts a logical address received in the writing operation to the physical address which is different from the physical address to which said logical address conversion means converted a logical address, identical to the logical address to be presently converted, in a preceding writing operation.

Interference No. 104,760

2. The claims of the parties which correspond to the count are:
Yamagami: 9 and 14
Harari: 63 and 64
3. Harari's claims 63 and 64 are identical to Yamagami's claims 9 and 14.
4. The involved Harari application (U.S. Serial No. 09/103,056) was filed on June 23, 1998.
5. The involved Yamagami patent (U.S. Patent No. 5,644,539) was filed on November 25, 1992 and issued on July 1, 1997.
6. Harari application claims 63 and 64 were copied from claims 9 and 14 of the Yamagami patent, subsequent to the filing of the Harari involved application.
7. Harari was accorded the benefit for purposes of priority of application Serial No. 07/337,566 filed April 13, 1989; application Serial No. 07/963,837 filed October 20, 1992; application Serial No. 08/249,049 filed May 25, 1994; and application Serial No. 08/931,133 filed September 16, 1997.

The subject matter of the count

8. The count in this interference is directed to a storage device which includes a flash memory which is a type of electrically erasable and programmable read-only memory or EEPROM.

9. A flash memory is nonvolatile and retains its memory even after the power is shut down.
10. The storage area on the flash memory is divided into a plurality of physical sectors with physical addresses.
11. In a writing operation, a logical address conversion means converts a logical address or virtual identification information of data into a physical address on the flash memory where the data is to be written.
12. The logical address conversion means converts a particular logical address to a physical address which is different from the physical address the particular logical address was converted to in a preceding write operation.
13. A memory controller receives the physical addresses from the logical address conversion means and writes the data into a respective sector of flash memory.

The Harari involved application

14. The Harari application (Exhibit 2006) discloses a system of integrated circuit Flash EEPROM chips which are under the control of a controller (page 2, lines 26-34).
15. The Flash EEPROM cells on a chip are organized into sectors.
16. An object of the invention in the involved Harari application is to provide a Flash EEPROM memory which remains reliable after enduring a large number of write/erase cycles (page 2, line 1 to 4).

17. One of the features of the invention of the Harari application is that it allows defect mapping at the cell level. A defective cell is replaced by a substitute cell from the same sector so that each time the defective cell is accessed, its bad data is replaced by the good data from the substitute cell (page 3, lines 26 to 29).
18. The Harari application discloses an apparatus that remaps defective cells so that the whole sector does not need to be thrown away (page 15, lines 18 to 21).
19. Each sector 401 is organized into a data portion 403 and a spare portion 405. The data portion 403 is space available to the user. The spare portion 405 is organized into an alternative defects data area 407, a defect map area 409, a header area 411 and others area 413 for use by a controller 31 to handle the defects and other overhead information (page 16, lines 23 to 32).
20. In a write operation, a comparator compares the location on the flash EEPROM which is about to be written against a defect pointer map (page 29, lines 15 to 17).
21. If a defective location is pointed to, a match will exist between the address of the defective location and the defect pointer address value in the defect pointer map (page 19, lines 21 to 22).
22. When this match occurs, the memory saves the bit which is about to be written into the alternative defect data file 517 (page 22, lines 3 to 6).

23. After the bytes have been loaded into the selected memory, the controller issues a program command to the memory device and initiates a write cycle (page 22, lines 8 to 11).
24. The Harari application discloses that the collection of bits that was flagged as defective and were saved in the alternative defects data file 517 is then written in memory at the alternative defects data locations (see figure 5) thereby saving the good bit values to be used in a subsequent read. Once these data groups are written and verified, the sector write is considered completed (page 23, lines 5 to 11).
25. When the number of defective cells has exceeded the cell defect mapping's capacity for that specific sector, the whole sector is remapped (page 23, lines 12 to 15).
26. The controller marks the sector as defective and maps it to another sector with the defect pointer for the linked sectors stored in a sector defect map (page 23, lines 19-23).
27. The defect map for defective sectors may be stored in the data area of the sector, but may also be located in the controller hardware or be a part of the Flash EEPROM memory (page 23, lines 29 to 31).
28. The controller compares an address given to it to access data with the defect map. If a match occurs, access to the defective sector is denied and the

corresponding substitute sector is accessed instead (page 23, lines 31 to 35).

29. The remapping can also be performed by the microprocessor. If the remapping is preformed by the microprocessor, the microprocessor looks at the incoming address and compares it against the sector defect map and if a match occurs, it substitutes the alternative location as the new command (page 24, lines 3 to 8).

The European reference

30. The disclosure of European Patent 0 392 895 A2 (Exhibit 2013)("European reference") is substantially the same as the disclosure of the involved Harari application (Yamagami Opposition to Harari Preliminary Motion No. 1, Fact No. 1; Kimura Declaration (Exhibit No. 2001, paragraph 43; Harari Reply No. 1, Fact No. 1).

Holzhammer

31. U. S. Patent No. 5,630,093 to Holzhammer (Exhibit 2014)("Holzhammer") discloses a storage device employing a flash memory array (col. 5, lines 8 to 10; col. 8, lines 5 to 10).
32. The flash memory is divided into a number of sectors (col. 4, lines 24 to 28).
33. A cluster mapping table 446, depicted in Figure 9, maps logical sectors called for by the personal computer system to the physical sectors of the flash memory array and thus forms a logical address conversion means (col. 15, lines 13 to 17).

34. A bad sector is one which contains a physical problem which prevents storage of data without errors (col. 18, lines 2 to 7).
35. The cluster map table 446 converts a logical sector called for by the personal computer system to a physical address on the flash memory which is different than the physical address previously associated with the same logical sector called for by the personal computer system in a previous writing operation. In table 446, the data in logical sector 2 called for by the personal computer system is mapped to physical sector 407. However, if physical sector 407 is a bad sector, data in logical sector 2, for example, is mapped to physical sector 443 (col. 17, line 64 to col. 18, line 63; col. 19, line 55 to col. 20, line 14).
36. A memory controller receives the physical address resulting from the conversion by the logical conversion means and writes data into a respective physical sector (col. 8, lines 14 to 41; col. 8, line 66 to col. 17, lines 16 to 20).
37. The cluster map table stores physical addresses of the physical sector into which data should be written in the next data writing operation. For example, because the physical sector 407 is a bad sector, the physical sector into which the data should be written in the next data writing operation is 443, which is stored in the cluster map table (col. 17, lines 29 to 40; col. 17, line 64 to col. 18, line 49; col. 19, line 55 to col. 20, line 14).

The declarations

The Kimura declaration

38. Yamagami has filed the declaration of Kiochi Kimura (Exhibit 2001) in support of the Yamagami preliminary motions.
39. Kimura states that the involved Harari application does not disclose or suggest the logical conversion means of the count which is included in the non-volatile memory device 29.
40. Kimura further states that as data is stored in the alternative defects file 517 an identical logical address is not converted to a different physical address than in a preceding writing operation.
41. In addition, Kimura states that the involved Harari application relates to the remapping of cells rather than sectors.
42. In regard to the European Reference, Kimura states that the European Reference does not disclose or suggest the invention recited in claims 9 and 14.
43. In regard to the Holzhammer reference, Kimura states that Holzhammer does not disclose or suggest the invention recited in claims 9 and 14 because two different logical addresses 2 and S are necessary to access two different physical addresses 407 and 421.

The Simko declaration

44. Harari has filed the declaration of Richard Simko (Exhibit 1003) in support of Harari preliminary motion 1 and the declaration of Richard Simko (Exhibit 1005) in support of Harari oppositions to Yamagami preliminary motions.
45. Simko states that the involved Harari application discloses a controller as the logical address conversion means in one embodiment and a microprocessor as the logical address conversion means in another embodiment.
46. Simko further states that the embodiment in the Harari application, wherein the microprocessor serves as the logical conversion means would have enabled one of ordinary skill in the art to make and use the invention where a microprocessor is included in the "storage device" as well.
47. In response to the statement in the Kimura declaration that data is not stored in a different physical location but in the alternative defects data file 417, Simko states that Kimura glosses over the last step in the writing process wherein the data stored in the alternative defects file is written in memory at the alternative defects data location (i.e. new physical address).

Discussion

Yamagami's Preliminary Motion number 1

This motion is entitled a "contingent" motion. However, the motion does not state the contingency. Therefore, we regard it as non-contingent.

The junior party has several sections in the motion with titles that state that there is no enabling disclosure for count 1 or Harari claims 63 and 64 as required by 35 U.S.C. § 112, first paragraph.¹

However, within these various sections of the motion, the junior party, in addition to arguing lack of enablement, argues that the involved Harari application does not disclose a written description of the subject matter of claims 63 and 64.² For example, at page 11, the junior party argues :

... the Harari Application (Ex 2006) does not satisfy the written description requirement of the first paragraph of 35 U.S.C. § 112 of the subject matter recited in Count 1 and copied claims 63 ...

In addition, the junior party argues at pages 2, and 20 to 23 of the motion that claims 63 and 64 add new matter which is tantamount to an argument that the Harari application lacks written description of the subject matter recited in claims 63 and 64. Further, the Kimura declaration (Exhibit 2001) states at page 2:

¹ Section 112 of 35 U.S.C. applies to the claims rather than the count. Therefore, we will regard this motion as being directed to claims 63 and 64 of the involved Harari application. Harari claim 63 is identical to one of the alternatives of count 1.

² The description requirement found in 35 U.S.C. § 112 is separate from the enablement requirement. See Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1562, 19 USPQ2d 1111, 1115 (Fed. Cir. 1991); In re Wilder, 736 F.2d 1516, 1520, 222 USPQ 369, 372 (Fed. Cir. 1984).

... the Harari application does not disclose or suggest the subject matter as per Count 1 logical address conversion means for converting of a logical address received in a present writing operation to a physical address. . .

In its preliminary motion, Yamagami also argues that Harari fails to provide a disclosure of the best mode contemplated by the Harari inventors at the time of the invention (page 8).

Accordingly, we interpret the junior party's arguments in the preliminary motion number 1 as directed to the written description requirement, the enablement requirement and the best mode requirement, despite the inaccurate headings used by Yamagami throughout its preliminary motion.³

Claim 63 recites:

A storage device employing a flash memory, wherein a storage area of said storage device is divided into a plurality sectors identified by physical addresses, said storage device includes;

logical address conversion means which receives a logical address of data in a data writing operation and converts said logical address into a physical address, and

a memory controller for receiving said physical address resulting from the conversion by the conversion means, and writing said data into a respective physical sector;

³ Note, that 37 CFR § 1.637(a) requires the movant to include in its motion, a statement of the precise relief requested.

wherein said logical address conversion means converts a logical address received in the writing operation to the physical address which is different from the physical address to which said logical address conversion means converted a logical address, identical to the logical address to be presently converted, in a preceding writing operation.

Written Description

A party moving for judgment on the ground that an opponent's claims corresponding to the count lack written description support in its involved application has the burden of submitting with the motion evidence which prima facie establish that the limitation or limitations in question lack either express or inherent support in the involved application. 37 CFR §§ 1.637(a); 1.639(a); Behr v. Talbott, 27 USPQ2d 1401, 1407 (Bd. Pat. App. & Int. 1992). Mere attorney argument will not suffice. Meitzner v. Mindick, 549 F.2d 775, 782, 193 USPQ 17, 22 (CCPA), cert. denied, 434 U.S. 854 (1977). The evidence may be in the form of patents, printed publications and affidavits. 37 CFR § 1.639(b).

The junior party argues that the phrases "logical address," "physical address," "logical address conversion means," "receives a logical address of data in a data writing operation and converts said logical address into a physical address" and "converts a logical address received in the writing operation to the physical address which is different from the physical address to which said logical address conversion means converted a logical address, identical to the logical address presently converted, in a

preceding writing operation" do not appear in the Harari application, and thus the specification fails to provide written description support for claim 63.

We do not find this argument to be persuasive because the test for determining compliance with the written description requirement is whether the disclosure of the application as originally filed reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter, rather than the presence or absence of literal support in the specification for the claim language. See Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1116-17 (Fed. Cir. 1991) and In re Kaslow, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983).

As such, the junior party has the burden of establishing that the Harari application does not reasonably convey to a person of ordinary skill in the art that the inventors had possession at the time of the later claimed subject matter rather than whether the exact words of the claim can be found in the Harari application.

The junior party argues that the involved Harari application does not disclose a storage device that includes a logical address conversion means which converts a logical address to a physical address. In the junior party's view, the involved Harari application discloses that the microprocessor rather than the controller 31 converts the logical address to a physical address and that it is only the controller 31 which is disposed in the storage device.

It is true that in one of the embodiments disclosed in the Harari application, it is the microprocessor which performs the logical address conversion operation. However, the Harari application discloses at pages 23 to 24 that in one embodiment, the controller 31 is given an address to access data, and it is the controller 31 that compares this address against the sector defect map and when a match occurs, access to the defective sector is denied and the substitute address present in the defect map is entered and the substitute sector is accessed. Therefore, in this embodiment, it is indeed the controller 31 that performs the logical address conversion. We note that Yamagami's own expert admits that the controller 31 performs a logical address to physical address conversion operation in one embodiment (Exhibit 2001, page 5, paragraph 13).

The junior party also argues that the involved Harari application does not disclose any element that performs the functions performed by the logical address conversion means recited in claims 63 and 64.

We do not agree. The Harari application discloses, as detailed above, that at least the controller performs the logical address conversion.

The junior party also argues that in the device of the involved Harari application, the logical address of the preceding write operation and the logical address of the present writing operation are the same and the physical address of the present writing

operation and the preceding writing operation are the same, namely all defective cells or sectors are written into the alternative defect register 517.

We agree with the junior party that the logical address of current and preceding writing operations are the same.⁴ However, while it is true that all of the data destined for defective cells is written into the alternative defect register 517 initially, the data is ultimately written into an alternative cell in the Flash EEprom. The Harari application discloses:

In addition, the collection of bits that was flagged as defective and were saved in the alternative defects data file 516 is then written in memory at the alternative defects data locations (see figure 5), thereby saving the good bit values to be used on a subsequent read. Once these data groups are written and verified, the sector write is considered completed. (page 23, lines 5 to 11).

In our view, Harari discloses a logical address conversion means that converts a logical address to an address in an alternative defects data file and then to a physical address in the Flash EEprom memory. In this regard, we observe that claim 63 does not recite that the logical address conversion means converts a logical address directly to a physical address which is different from the physical address of the preceding writing operation.

⁴ We note that at page 2 of the Harari application, it is disclosed that the flash memory is subjected to numerous write cycles.

The junior party further argues that the writing operation disclosed in the Harari application when the sector defect map is used is to a cell identified by the corrected address information, and not to a physical sector identified by a physical address as recited in claim 63.

This is simply not true. At page 23, Harari discloses that when the number of defective cells in the sector has exceeded the cell defect mapping capacity for that specific sector, the controller marks the sector as defective and maps it to another sector. In this way, the data destined for a defective sector is written instead into a substitute sector.⁵ The sector defect map can be located in a spare area of the original defective sector or located in the controller hardware or be part of the Flash EEprom memory. In addition, as Yamagami discloses that an object of the invention is to provide a Flash EEprom memory system that remains reliable after enduring a large number of write cycles, it is implicit in the disclosure of the involved Harari application that there are successive write operations.

In view of the foregoing, it is our determination that the junior party has failed to meet its burden of establishing that the involved Harari application disclosure does not

⁵ We note that when sector remapping is done, the defective sector is not accessed but rather the substitute sector (which is different than the sector accessed in a preceding write operation) is accessed instead.

provide a written description of the subject matter of claim 63 as required by 35 U.S.C. § 112.

Yamagami argues that there is no disclosure of the subject matter of claim 64 because the Harari application does not disclose or suggest the features recited in claim 63, and as such, does not disclose or suggest the features of claim 64 which is dependent on claim 63. In addition, Yamagami argues that claim 64 recites that the write sector pointer is a further element of the storage device, not an element which forms a part of the logical address to physical address conversion means.

Claims 64 recites:

A storage device employing a flash memory according to claim 63, further comprising:
a write sector pointer for storing said physical address of the physical sector into which data should be written in the next data writing operation,
wherein said logical address conversion means converts said logical address into said physical address stored in said write sector pointer.

As we detailed above in our discussion of the written description of the subject matter of claim 63, it is our opinion that the junior party has failed to prove that the involved Harari application does not describe the features of claim 63. In addition, we agree with the senior party that the involved Harari application does disclose a write sector pointer in the form of defect pointers at page 23, lines 19 to 20. These defect pointers, which correspond to addresses for substitute sectors (the sector into which

data should be written in the next data writing operation) are stored in the sector defect map. This sector defect map may be stored in another memory maintained by the controller or in the original defective sector and thus not form a part of the controller which forms the logical address physical address conversion means (page 23, lines 27 to 31).

Enablement

The junior party argues that the Harari application fails to enable a person of ordinary skill in the art to make and use the subject matter of claim 63. To prevail on a motion for judgment that a party's application lacks an enabling disclosure, the moving party must show that the disclosure would not enable a person of ordinary skill in the art to make or use the invention without undue experimentation on their part. See In re Donohue, 550 F.2d 1269, 1271, 193 USPQ 136, 137 (CCPA 1977). The burden of proof is on the moving party who must show lack of enablement by a preponderance of the evidence. Kubota v. Shibuya, 999 F.2d 517, 519 n.2, 27 USPQ2d 1418, 1421 n.2 (Fed. Cir. 1993); Field v. Knowles, 183 F.2d 593, 596, 86 USPQ 373, 375 (CCPA 1950).

In regard to the lack of enablement argument, Yamagami addresses what is actually disclosed in the Harari application, but fails to include a discussion of whether a person could make or use the invention without undue experimentation.

The mere absence of disclosure does not per se establish lack of enablement. An inventor need not explain every detail since the inventor is speaking to those skilled in the art. In re Howarth, 654 F.2d 103, 105, 210 USPQ 689, 691 (CCPA 1981). Rather, the question is whether a person of ordinary skill in the art coupled with knowledge known in the art would have been enabled to make and use the invention without undue experimentation.

As the junior party has not addressed whether a person skilled in the art could make or use the invention without undue experimentation, this portion of the motion fails because the junior party has failed to meet its burden.

Best Mode

Yamagami also argues that the Harari application fails to disclose a best mode. The best mode provision of § 112 speaks in terms of the best mode "contemplated by the inventor," there is no objective standard by which to judge the adequacy of the best mode disclosure. Instead, only evidence of "concealment," whether accidental or intentional, is considered. DeGeorge v. Bernier, 768 F.2d 1318, 1324, 226 USPQ 758, 763 (Fed. Cir. 1985). The specificity of the disclosure required to comply with the best mode requirement must be determined by the knowledge of the facts within the possession of the inventor at the time of the filing of the application. See United States Dep't of Energy v. Daugherty, 687 F.2d 438, 446, 215 USPQ 4, 11 (CCPA 1982).

Yamagami has not discussed what mode of practicing the invention was regarded by Harari as best. In addition, Yamagami has failed to address the issue of concealment. As such, this portion of this motion fails.

In view of the foregoing, the junior party's preliminary motion for a judgment pursuant to CFR § 1.633(a) that claims 63 and 64 of the Harari application are unpatentable is denied.

Yamagami's Preliminary Motion number 2

This motion is entitled a "contingent" motion. However, the motion does not state the contingency. Therefore, we regard this motion as non-contingent.

Yamagami's preliminary motion number 2 seeks to designate claim 14 as not corresponding to the count.

Claim 14 recites:

A storage device employing a flash memory according to claim 9, further comprising:
a write sector pointer for storing said physical address of the physical sector into which data should be written in the next data writing operation,
wherein said logical address conversion means converts said logical address into said physical address stored in said write sector pointer.

Yamagami has the burden of proving that claim 14 of the Yamagami patent does not define the same patentable invention as any Harari claims ("designated claims") designated in the notice declaring the interference as corresponding to the count that

Yamagami does not dispute. 37 CFR § 1.637(c)(4)(ii). Section 1.601(n) of 37 CFR reads in pertinent part as follows:

...Invention "A" is a *separate patentable invention* with respect to invention "B" when invention "A" is new (35 U.S.C. 102) and non-obvious (35 U.S.C. 103) in view of invention "B" assuming invention "B" is prior art with respect to invention "A".

Therefore, Harari's designated claims are treated as prior art for purposes of this analysis.

Mere reference to a claimed feature which is not disclosed by the prior art and not included in the Count does not per se establish "separate patentability" within the meaning of § 1.601(n). Rather, the question is whether the inclusion of the feature would have rendered the claim nonobvious to a person of ordinary skill in the art. See L'Esperance v. Nishimoto, 18 USPQ2d 1534, 1538 (Bd. Pat. App. Int. 1989).

Therefore, Yamagami has the burden of establishing, by a preponderance of the evidence, that its claim 14 is patentably distinct with respect to each of Harari's involved claims in accordance with the guidance set forth in Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966); 37 CFR § 1.637(c)(4)(ii); § 1.601(n).

Yamagami's motion is misdirected to whether the examiner in the interference memo established that the subject matter recited in claim 14 would have been obvious. Claim 14 was designated as corresponding to the count in the interference declaration issued by the Administrative Patent Judge ("APJ") that declared this interference. As

such, the designation of claim 14 as corresponding to the count was an interlocutory order issued by the APJ which is presumed correct. The burden of showing that an interlocutory order should be modified is on the party attacking the order. 37 CFR § 1.655(a). Yamagami, as the movant, bears the burden to prove that the subject matter recited in claim 14 is not the same or obvious over each of Harari's involved claims. This Yamagami has not done.

In response to the examiner's determination that U.S. Patent No. 4,829,425 to Bain ("Bain") discloses write pointers, Yamagami argues that a write sector pointer for storing a physical address of the physical sector into which data should be written in the next writing operation as set forth in claim 14, is not suggested or taught by the count (which is identical to Harari's claim 63) or the Bain reference. Yamagami further argues that Bain does not address a next data writing operation and has no discussion of a write sector pointer in combination with logical address conversion means that converts the logical address into the physical address stored in the write sector pointer as set forth in claim 14.

However, even if a feature is not taught in the prior art, Yamagami still must establish that the inclusion of the feature would not have been obvious to a person of ordinary skill in the art. While Yamagami argues in a conclusory matter that there is no evidence of a motivation to combine the Bain register set pointers with the subject matter of Harari's claim 63, Yamagami has not met its burden that there is no

motivation to make the combination. In fact, Yamagami has not discussed the set pointers of Bain in any detail.

Yamagami concludes that as there is no showing by the examiner that Yamagami claim 14 is the same invention as Harari claim 63, Yamagami claim 14 should be designated as not corresponding to the count. As discussed above, the analysis fails to sufficiently meet Yamagami's burden to establish that claim 14 is not the same invention as Harari claim 63. It is Yamagami who must demonstrate nonobviousness. A lack of showing by the examiner of the opposite does not make the case for Yamagami.

In response to the senior party's argument in the opposition to this motion that Holzhammer discloses write sector pointers, Yamagami merely argues that Holzhammer does not disclose or suggest the conversion of a logical address which is different from the physical address to which the same logical address is converted in a preceding writing operation. However, this subject matter is recited in Harari claim 63. Yamagami concludes in the reply that Holzhammer does not disclose or suggest the subject matter of claim 14. The only portion of the reply which is directed to the combination of Holzhammer and the subject matter of Harari claim 63 is a conclusory statement that there is no showing of how the respective features of Holzhammer can be combined with the count (which is the same as Harari claim 63). Yamagami does

not discuss in any meaningful way why the teachings of Holzhammer cannot be combined with the subject matter of the Harari claim 63.

In response to the senior party's argument in the opposition to this motion that the European reference discloses write sector pointers, Yamagami argues in the reply that the European reference does not disclose or suggest a write sector pointer for storing the physical address of the physical sector into which data should be written in the next writing operation. Yamagami has not addressed what the combination of the European reference and Harari claim 63 would suggest to a person of ordinary skill. Yamagami merely states that there is no showing of how the European reference may be combined with the subject matter of Harari claim 63 or the motivation to make such a combination. The problem, however, is that it is Yamagami who has to make a showing of the opposite.

Furthermore, Yamagami makes no representation that it is not aware of any additional prior art which would render obvious Yamagami claim 14 when taken in view of a Harari claim designated as corresponding to the count in light of the additional prior art. The absence of such representation, is an additional ground of why Yamagami has not sustained its burden of proving that its claim 14 should not correspond to the count.

This motion is denied because Yamagami has failed to meet its burden of establishing that the subject matter of claim 14 would not have been obvious in view of

Interference No. 104,760

the subject matter of those involved Harari claims whose correspondence to the count Yamagami does not dispute.

Yamagami's Preliminary Motion number 3

Yamagami's preliminary motion number 3 seeks an order according benefit for purposes of priority of earlier filed applications: Japanese Patent Application No. 3-310848, filed November 26, 1991; Japanese Patent Application No. 3-314297, filed November 28, 1991 ; Japanese Patent Application No. 4-031756, filed February 19, 1992 and Japanese Patent Application No. 4-099891, filed April 20, 1992 under 37 CFR § 1.633(f). This motion is unopposed. The motion is granted.

Yamagami's Preliminary Motion number 4

In this preliminary motion, Yamagami attacks the benefit accorded Harari in the notice declaring this interference of : U.S. Patent Application Serial No. 07/337,566; U.S. Patent Application Serial No. 07/963,837; U.S. Patent Application Serial No. 08/249,049; and U. S. Patent Application Serial No. 08/931,133. Yamagami argues that the subject matter of claims 63 and 64 is not disclosed in the Harari benefit applications in such a matter as to enable a person of ordinary skill to make or use the invention. In this motion, like in preliminary motion number 1, Yamagami has failed to address the issues of whether a person of ordinary skill in the art could make or use the invention without undue experimentation and as such has failed to establish that a

person of ordinary skill in the art would not have been enabled by the above-listed benefit applications. As such, this motion is denied.

Yamagami's Preliminary Motion number 5

This motion is entitled a "contingent" motion. However, the motion does not state the contingency. Therefore, we will regard it as noncontingent.

Yamagami's preliminary motion number 5 seeks to redefine the interfering subject matter by an order stating that claims 65 and 66 of the involved Harari application correspond to the count. This motion is unopposed. This motion is granted.

Yamagami's Contingent Preliminary Motion number 6

Yamagami's preliminary motion number 6 seeks a judgment that Harari claims 65 and 66 are unpatentable and is contingent upon the granting of Yamagami's preliminary motion number 5. Yamagami's argument is that since the involved Harari application lacks an enabling disclosure of the subject matter of claim 63 from which claims 65 and 66 depend, the Harari application lacks an enabling disclosure of the subject matter of claims 65 and 66 as well. In view of the junior party's failure to prove that the involved Harari application does not provide a disclosure that satisfies both the written description and enablement requirement of 35 U.S.C. § 112, first paragraph, with regard to claim 63 as set out in detail in our discussion of Yamagami's preliminary motion number 1, this motion is denied.

Yamagami's Contingent Preliminary Motion number 7

Yamagami's preliminary motion number 7 attacks the benefit afforded Harari in the notice declaring the interference and is contingent upon the granting of Yamagami's preliminary motion number 5. Yamagami argues that claims 65 and 66 are not entitled to the benefit of the filing dates of: Application Serial No. 07/337,566, filed April 13, 1989; Application Serial No. 07/337,566, filed April 13, 1989; Application Serial No. 07/963,837, filed October 20, 1992; Application Serial No. 08/249,049, filed May 25, 1994; and Application Serial No. 08/931,133, filed September 16, 1997. Yamagami reasons that since the involved Harari application does not include an enabling disclosure of claims 65 and 66, the Harari benefit applications likewise do not include an enabling disclosure since the Harari benefit applications are similar in content to the involved Harari application.

However, the issue is not whether the benefit applications include an enabling disclosure of the subject matter of claims 65 and 66, rather the issue is whether the benefit applications describe an embodiment within the scope of the count. Hunt v. Treppschuh, 523 F.2d 1386, 1389, 187 USPQ 426, 429 (CCPA 1975); see also Weil v. Fritz, 572 F.2d 856, 865 n.16, 196 USPQ 600, 608 n.16 (CCPA 1978). An earlier filed application need not describe all species the count encompasses. Utter v. Hiraga, 845 F.2d 993, 998, 6 USPQ2d 1709, 1714 (Fed. Cir. 1988). Therefore, in order for Yamagami to establish that claims 65 and 66 are not entitled to the filing date of

Interference No. 104,760

Application Serial No. 07/337,566, filed April 13, 1989, Yamagami must prove that Application Serial No. 07/337,566 does not describe an embodiment within the scope of the count. Such proof is also necessary to establish that Harari is not entitled to the filing dates of: Application Serial No. 07/963,837, filed October 20, 1992; Application Serial No. 08/249,049, filed May 25, 1994; and Application Serial No. 08/931,133, filed September 16, 1997. We note that Yamagami has not addressed the disclosures of the above-listed benefit applications with regard to Harari claims 63 and 64 which recite embodiments within the scope of the count.

Yamagami has not shown that the earlier filed Harari applications do not describe an embodiment within the scope of the count. As such, this motion is denied.

Yamagami's Contingent Preliminary Motion number 8

In this preliminary motion, Yamagami seeks a judgment that claims 63 and 64 of the involved Harari application are unpatentable based upon the granting of Yamagami's preliminary motion number 4. In preliminary motion number 4, Yamagami attacks the benefit accorded Harari in the notice declaring the interference of U.S. Applications Serial Nos. 07/337,566; 07/963,837; 08/249,049 and 08/931,133. In preliminary motion number 8, Yamagami reasons that if Harari claims 63 and 64 are not accorded the benefit of the filing dates of the above noted applications, the Yamagami patent is prior art to Harari claims 63 and 64. We note that Yamagami has confused benefit for the purposes of establishing priority of invention (35 U.S.C. § 119) with

benefit for purposes of establishing patentability over prior art (35 U.S.C. § 120). In any case, as preliminary motion number 4 was denied and therefore, the contingency did not materialize, Yamagami's contingent preliminary motion number 8 is dismissed.

Harari's Preliminary Motion number 1

In Harari's preliminary motion number 1, Harari seeks judgment under 37 CFR § 1.633(a) because in Harari's view, the Yamagami claims 9 and 14 are unpatentable under 35 U.S.C. § 102(b) as anticipated by the European Patent Application Publication No. 0 392 895 A2 (Harari Exhibit 1001)("European patent") and Holzhammer.⁶

Harari argues that claims 9 and 14 of the Yamagami patent are anticipated by the European patent. Yamagami has admitted that the disclosure of the European patent is substantially the same as the Harari application (Yamagami's Opposition to Harari preliminary motion number 1, Fact No. 1).

In response to this motion, Yamagami argues that the European patent does not anticipate Yamagami claims 9 and 14. Yamagami argues that the European patent does not disclose that the logical address conversion means is disposed in the storage device and that the European patent relates to cell remapping rather than sector remapping. Yamagami also argues that the European patent does not explicitly or

⁶ Holzhammer and the European patent are not prior art to Harari.

implicitly disclose a storage device employing a flash memory, wherein a storage area of the storage device is divided into a plurality of physical sectors identified by physical addresses. Further, Yamagami argues that the European patent does not disclose explicitly or implicitly conversion of a logical address of a present writing operation to a physical address different from the physical address converted from the logical address in a preceding writing operation. These are the same arguments Yamagami made in its preliminary motion number 1 in regard to the involved Harari application. We refer the parties to that discussion for details of our opinion in this regard.

We are of the opinion that the European patent discloses sector remapping (Exhibit 1001, col. 2, lines 10 to 13; col. 5, lines 9 to 14; col. 6, lines 11 to 13 and 17 to 20; col. 15, lines 17 to 20). In addition, the European patent discloses a logical address conversion means disposed in a storage device (Exhibit 1001, col. 15, lines 24 to 50). Although the data is temporarily stored in the alternative defects data file 517, it is ultimately stored in memory at the alternative data defects location which is a different physical address converted from the logical address in the preceding writing operation. Therefore, the European patent does disclose conversion of a logical address of a present writing operation to a physical address different from the physical address converted from the logical address in a preceding writing operation.

In regard to Holzhammer, we agree with the senior party that Holzhammer discloses the subject matter of Yamagami's claims 9 and 14.

Yamagami argues that Holzhammer discloses that a first logical address is converted to a first physical address and that a second subsequent different logical address is converted to a second different physical address in a subsequent conversion step. We do not agree.

Holzhammer discloses at column 18, lines 32 to 58 that logical address 2 is converted to physical address 407 in a first conversion operation and to physical address 443 in a subsequent conversion operation.

Yamagami also argues that there is no disclosure in Holzhammer of memory controller as is recited in Yamagami claim 9.

We do not agree. Holzhammer discloses a controller 92 which controls the structure of the flash memory array (col. 8, line 66 to col. 9, line 5).

In regard to claim 14, Harari argues that since the cluster mapping table 446 seen in Figure 9 is a table comprised of a plurality of linked-list entries associating logical addresses with physical addresses, Holzhammer discloses a write sector pointer which stores the physical address of the physical sector into which data should be written in the next data writing operation, as recited in claim 14.

Yamagami argues that the cluster mapping table 446 in Holzhammer maps a logical address to a logical address and that the physical address is not stored in the cluster mapping table 446.

As seen in Figure 9, this is not true. A logical address 2 is converted to physical addresses 407 and 443 e.g. and the physical addresses are indeed stored on the cluster mapping table 446. As such, we agree with the senior party that Holzhammer does indeed disclose a write sector pointer.

The motion is granted.

**Harari's Responsive Preliminary Motion number 2 and
Contingent Preliminary Motions 3 and 4**

In Harari's responsive preliminary motion number 2, Harari seeks to add claims 67 and 68 in an attempt to eliminate the arguments posed in Yamagami's preliminary motion numbers 1, 4 and 6. In view of our denial of Yamagami's preliminary motion numbers 1, 4 and 6, we dismiss Harari's preliminary motion number 2.

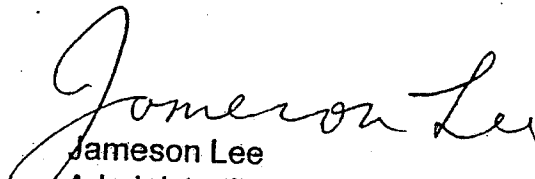
Harari's preliminary motions numbers 3 and 4, which are contingent upon the granting of Harari preliminary motion number 2 and Yamagami's motion numbers 1, 4 and 6, which were all denied, are dismissed.


Order to Show Cause

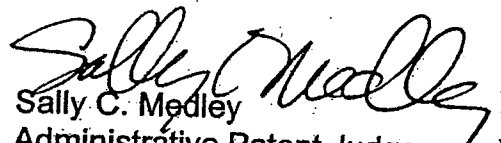
The preliminary statements are open on the record. According to the preliminary statements, Harari's filing date, which is a constructive reduction to practice, is April 13, 1989, while Yamagami's conception as well as reduction to practice date is November

Interference No. 104,760

26, 1991. Therefore, Yamagami is given **twenty days (20)** from the date of this paper to show cause why judgment should not be entered against Yamagami.


Jameson Lee
Administrative Patent Judge


Murriel E. Crawford
Administrative Patent Judge


Sally C. Medley
Administrative Patent Judge

) BOARD OF PATENT
) APPEALS
) AND
) INTERFERENCES

MEC/tdl

Interference No. 104,760

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**DECISION ON YAMAGAMI SECOND REQUEST FOR
RECONSIDERATION AND FINAL JUDGMENT, PATENT
INTERFERENCE NO. 104,760**

The opinion in support of the decision being entered
today is not binding precedent of the Board

Filed by: Trial Section Merits Panel
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Paper No. 97

Filed
29 May 2003

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

HAJIME YAMAGAMI, KOUICHI TERADA, YOSHIHIRO HAYASHI,
TAKASHI TSUNEHIO, KUNIHIRO KATAYAMA,
KENICHI KHAKI, and TAKESHI FURUNO,
Junior Party,
(Patent 5,644,539),

v.

ELIYAHOU HARARI, ROBERT D. NORMAN and
SANJAY MEHROTRA,
Senior Party,
(Application 09/103,056).

Patent Interference No. 104,760

Before LEE, CRAWFORD and MEDLEY, Administrative Patent Judges.

MEDLEY, Administrative Patent Judge.

**DECISION ON YAMAGAMI SECOND REQUEST FOR RECONSIDERATION
AND FINAL JUDGMENT**

A. Introduction

A decision on preliminary motions was entered 18 April 2003. In our decision, Yamagami was ordered to show cause why judgment should not be entered against it (Paper 91 at 35). In response to the show cause order, Yamagami filed a request for reconsideration of our decision on preliminary motions (Paper 93). Yamagami's request for reconsideration was dismissed for procedural errors, without prejudice to file another request for reconsideration (Paper 94).

On 20 May 2003, Yamagami filed a second request for reconsideration (Paper 95). Yamagami seeks reconsideration of that part of our decision on preliminary motions in which we (1) denied Yamagami Preliminary Motion 1 for judgment against Harari based on 35 U.S.C. § 112, ¶ 1, and (2) granted Harari Preliminary Motion 1 for judgment against Yamagami on the grounds that Yamagami's involved claims are unpatentable based on prior art.

B. Discussion

A party requesting reconsideration of an interlocutory decision must specify with particularity points believed to have been misapprehended or overlooked in rendering the decision. 37 CFR § 1.640(c). A request for reconsideration is not a new opportunity to raise issues which should have been raised during the preliminary motions period. Further, a request for reconsideration will not be granted where the moving party merely disagrees with the decision of the panel.

Yamagami argues that we overlooked or misapprehended Yamagami's arguments and evidence of record that Harari did not provide written description support for Harari claims 63

and 64 (Recon.¹ 2). In essence, Yamagami asserts that we did not consider that portion of Yamagami preliminary motion 1 where Yamagami argued that Harari lacked written description support for Harari claims 63 and 64. However, as is evident from our seven page discussion addressing Yamagami's written description arguments, the panel did consider Yamagami's arguments and the evidence that Yamagami directed us to in support of its arguments.

Yamagami, as the requestor for reconsideration of our decision on preliminary motions, must demonstrate how we specifically misapprehended or overlooked an argument made, or evidence relied upon in support of an argument. A general argument such as that made by Yamagami does not provide a basis upon which relief will be granted.

Yamagami argues that there is insufficient detailed description of how to make or use the controller 31 to perform the claimed conversion with respect to sector remapping (Recon. 3-4). Yamagami argues that it set forth this point in its preliminary motion through certain Material Facts, in its argument section of the motion, in certain paragraphs of the Kimura declaration, and in its reply ¹² (Recon. 3-4). We find no such argument made by Yamagami in the argument section of its preliminary motion 1. To the extent that Yamagami now directs us to statements of facts in Yamagami preliminary motion 1 and passages in the Kimura declaration in support of the new argument, it is too late. We note that in the argument section of Yamagami preliminary motion 1, there is not a single citation to the Kimura declaration, or to any statement of fact. It is

¹ Recon. refers to Yamagami's second request for reconsideration, i.e. Paper 95.

² In its request for reconsideration, Yamagami argues that it raised the issue on page 5, line 29 thru page 7. (Recon. 4). We assume that Yamagami is referring to its reply 1, since the reply 1 matches the description given by Yamagami.

not the role of the board to play detective with a party's evidence or statements of facts and come up with an argument for the party. That is the role of counsel, not judge. Yamagami should have directed our attention to any statements of facts or to paragraphs of the Kimura declaration in its argument section of its motion. It is too late for Yamagami to do so now. Note further, that incorporation by reference of arguments is not permitted. See Paper 1, Standing Order § 13. Furthermore, in deciding Yamagami preliminary motion 1, we did not consider Yamagami's reply. Because Yamagami's preliminary motion 1 failed to set forth a prima facie case for entitlement to relief, Harari's opposition to Yamagami's preliminary motion 1 was not considered. Consequently, Yamagami's reply need not have been considered. In any event, we have considered the statements of facts, paragraphs in the Kimura declaration and arguments made in Yamagami reply that Yamagami now direct us to and do not find the argument now advanced, i.e. that there is insufficient detailed description of how to make or use the controller 31 to perform the claimed conversion with respect to sector remapping.

Yamagami argues that our statement on page 17, lines 2-11 of our decision that we note that Yamagami's own Expert admits that the controller 31 performs a logical address to a physical address conversion operation in one embodiment (Exhibit 2001, page 5, paragraph 13) is not true. Yamagami argues that there is no admission by Kimura at any point in his declaration (Recon. 4). We agree that paragraph 13 of the Kimura declaration does not support the statement made in our decision. Accordingly, we modify the decision, by deleting lines 8-11 on page 17, beginning with We note.... The change to our decision to delete the above noted sentence, however, does not change the overall outcome of our decision to deny Yamagami preliminary motion 1.

Yamagami argues that the panel erred when it attributed the stated feature in the Harari specification of providing a flash EEPROM memory which remains reliable after enduring a large number of write/erase cycles to cell and sector defect re-mapping. Yamagami argues that Harari's sector remapping is conditional, in that it only occurs after a defective sector is detected and would not satisfy the written description requirement for prolonging life (Recon. 4-5).

There are several problems with Yamagami's argument. First, we did not attribute reliability to the sector remapping embodiment. We said in our decision that as Yamagami discloses that an object of the invention is to provide a Flash EEPROM memory system that remains reliable after enduring a large number of write cycles, it is implicit in the disclosure of the involved Harari application that there are successive write operations. Yamagami does not argue that Harari does not perform successive write operations, or that the sector remapping is not performed in two consecutive write operations. Rather, Yamagami argues that the remapping (conversion) is not done every time there is a write operation.

Yamagami made this argument in its reply 1 (Reply 1 at 6, lines 4-6) and in its opposition to Harari's preliminary motion 1. However, in deciding Yamagami's preliminary motion 1, we did not consider Yamagami's reply or Yamagami's opposition to an unrelated motion. Because Yamagami's preliminary motion 1 failed to set forth a prima facie case for entitlement to relief, Harari's opposition to Yamagami's preliminary motion 1 was not considered. Consequently, Yamagami's reply need not have been considered. That Yamagami made the argument in an opposition to an unrelated motion is without merit. We will not, at this late stage in the proceedings, consider arguments Yamagami made in an unrelated opposition to an unrelated motion. Moreover, as stated above, incorporation of arguments is not permitted.

In any event, we note that Harari claims 63 and 64 are not limited to performing a conversion for every write operation. The claims are broad enough to include performing a conversion at some point in time between two consecutive write operations. Furthermore, lacking from the claim language of Harari claims 63 and 64 is a requirement that the conversion act to prolong the life of the memory.

Yamagami argues that we misapprehended or overlooked statements made by Kimura and arguments advanced by Yamagami in its preliminary motion 1 that it is inherently obvious that undue experimentation (although this term is not specifically used) would be required to practice the apparatus as disclosed in the Harari specification ... (Recon. 5). As stated above, Yamagami does not, in the argument section of Yamagami preliminary motion 1, direct our attention to any passage in the Kimura declaration. Yamagami cannot now direct us to passages in the Kimura declaration with the hopes that we will consider those passages. It is too late. Consideration of such evidence would be prejudicial to Harari. In any event, it is not enough to allege, or for a declarant to state that experimentation would be required to practice an invention, or even that undue experimentation would be required without sufficient supporting evidence to back up the argument or statement.

Yamagami argues that we erred in not giving deference to the examiner's determination that Yamagami's claims were patentable over the subject matter of the European patent application and Holzhammer (Recon. at 5). We are not bound by decisions made by an examiner during ex parte prosecution. During an interference, independent review of issues are made. See Glaxo Wellcome, Inc. v. Cabilly, 56 USPQ2d 1983, 1984 (BPAI (ITS)). (Neither the Board nor a party are bound by an ex parte decision made during prosecution by another party.

A motion in an interference is not an appeal from the examiner's decision, but an independent request to the Board). Accordingly, we did not overlook the examiner's determination made during ex parte prosecution of the Yamagami involved patent. Instead, we reviewed Harari preliminary motion 1, Yamagami opposition 1, and the evidence related to the motion and opposition in making our decision.

Yamagami argues that we failed to mention, in our decision, that Harari has a burden to overcome in order for it to prove anticipation (Recon. 6). It is not necessary for an opinion to state the obvious. Rule 637(a) provides that the movant bears the burden to demonstrate that it is entitled to the relief requested. That we did not quote the rule in our decision does not mean that Harari was exempt from meeting its burden of proof. Yamagami has failed to sufficiently demonstrate that we ignored the burden in rendering our decision. By addressing Yamagami's opposition 1, it is inherent that the panel determined that Harari met its burden to demonstrate that it was entitled to the relief requested in the first place. Accordingly, we see no reason to amend our decision.

Yamagami disagrees with our determination that the European patent discloses sector remapping. Mere disagreement with a determination made by the panel is insufficient reason to grant a request for reconsideration.

Having considered Yamagami's arguments in its request for reconsideration, we grant Yamagami's request for reconsideration with respect to that portion of our decision on page 17, lines 8-11, by deleting the following: [w]e note that Yamagami's own expert admits that the controller 31 performs a logical address to physical address conversion operation in one

embodiment (Exhibit 2001, page 5, paragraph 13). As noted above, the deletion does not change our decision to deny Yamagami preliminary motion 1.

Having considered Yamagami's additional arguments, we conclude that Yamagami has failed to demonstrate that we misapprehended or overlooked any fact or argument first presented prior to the filing of the request for reconsideration. Accordingly, Yamagami's request for reconsideration is **granted-in-part**.

Since Yamagami is a junior party who has failed to overcome the effective filing date of the senior party Harari, judgment is entered against Yamagami.

Upon consideration of the record, it is

ORDERED that Yamagami's request for reconsideration is **granted-in-part**;

FURTHER ORDERED that judgment as to Count 1 (Paper 1 at 5), the sole count in the interference, is awarded against junior party HAJIME YAMAGAMI, KOUICHI TERADA, YOSHIHIRO HAYASHI, TAKASHI TSUNEHIO, KUNIHIO KATAYAMA, KENICHI KHAKI, and TAKESHI FURUNO;

FURTHER ORDERED that junior party HAJIME YAMAGAMI, KOUICHI TERADA, YOSHIHIRO HAYASHI, TAKASHI TSUNEHIO, KUNIHIO KATAYAMA, KENICHI KHAKI, and TAKESHI FURUNO is not entitled to a patent containing claims 9 and 14 (corresponding to Count 1) of patent 5,644,539;

FURTHER ORDERED that a copy of this paper shall be made of record in files application 09/103,056 and U.S. Patent 5,644,539;

FURTHER ORDERED that if there is a settlement agreement, attention is directed to
35 U.S.C. § 135 (c) and 37 CFR § 1.661.

JAMESON LEE
Administrative Patent Judge

MURRIEL E. CRAWFORD
Administrative Patent Judge

SALLY C. MEDLEY
Administrative Patent Judge

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DECISION ON APPEAL, APPEAL NO. 2001-1272

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 29

MAILED

UNITED STATES PATENT AND TRADEMARK OFFICE

SEP 27 2002

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

PAT. & T.M. OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ELIYAHOU HARARI, ROBERT D. NORMAN,
and SANJAY MEHROTRA

Appeal No. 2001-1272
Application No. 09/056,398

ON BRIEF¹

Before RUGGIERO, BLANKENSHIP, and SAADAT, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 63-67, which are all the claims remaining in the application.

We reverse.

¹ Appellants waived oral hearing (Paper No. 28).

BACKGROUND

The invention relates to programming and erasing of electronically erasable programmable read only (EEPROM) cells. Claim 63 is reproduced below.

63. A method of treating at least one erased EEPROM cell, comprising:

a) accessing a number of control gates and accessing a bit line, thereby activating a number of memory cells, each of said memory cells having a source, a drain, and a control gate;

b) subsequent to accessing said bit line, sensing the presence of at least one activated cell from said number of memory cells that is erased to a state other than one of at least two data states; and

c) subsequent to sensing the presence of said erased cell, applying a first voltage to said bit line, a second voltage to said control gate of at least said erased cell, and a third voltage to said source of at least said erased cell, said first and second voltages being higher than said third voltage.

Claims 63-67 stand rejected under 35 U.S.C. § 112, first paragraph.

We refer to the Final Rejection (Paper No. 16) and the Examiner's Answer (Paper No. 22) for a statement of the examiner's position and to the Brief (Paper No. 21) and the Reply Brief (Paper No. 23) for appellants' position with respect to the claims which stand rejected.

OPINION

At the outset, we note our agreement with appellants (e.g., Brief at 4) that the issue in the instant appeal is whether or not the instant claims pass muster under 35 U.S.C. § 112, first paragraph. In the instant proceeding, it is irrelevant whether or not a

claim before us defines the same patentable invention as a claim in the U.S. patent with which appellants have requested an interference. We thus make our determinations independent of any inquiry into whether the instant application and the patent claim interfering subject matter.

The initial statement of the rejection (Answer at 2) could be interpreted as being based on an alleged lack of enablement for the claimed subject matter. However, in view of the discussion between the examiner and appellants, we conclude that the rejection is based on an alleged lack of written description support for the subject matter now claimed.

We further note that the initial statement of the rejection alleges lack of support for language that does not appear in the claims before us. Since our review of the rejection is confined to the requirements of 35 U.S.C. § 112, first paragraph, we find the allegations that the disclosure does not provide support for language that is not in the claims to be misplaced. The disclosure need not provide support for language that is not in the claims.

In any event, the "Response to Argument" section of the Answer (at 2-5) asserts that steps (b) and (c) of claim 63 are not supported by the instant disclosure. Appellants' position (Brief at 4-6) is that the steps are described in a preliminary amendment to the written description and in instant Figure 23, added by the preliminary

amendment.² In particular, appellants refer (Brief at 5) to material describing "another feature of the invention," in which, subsequent to the erasing of a memory cell, the cell is "programmed slightly" to bring the cell to the state with the lowest threshold level (ground state) adjacent to the "erased" state. Appellants assert that claimed steps (b) and (c) correspond to steps 4 through 6 of Figure 23.

The examiner responds (Answer at 3-4) that the verification of step 5 is to check whether or not the addressed cells reach the program state, not the "erased" state. In the examiner's view, it follows that the voltages recited in step (c) are not applied, because the claim requires that the voltages be applied "subsequent to sensing the presence of said erased cell."

To comply with the "written description" requirement of 35 U.S.C. § 112, first paragraph, an applicant must convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention. The invention is, for purposes of the "written description" inquiry, whatever is now claimed. Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991).

The invention claimed does not have to be described in ipsis verbis in order to satisfy the description requirement of 35 U.S.C. § 112, first paragraph. Union Oil Co. v.

² Although couched in terms of the "effective filing date of the present application," apparently the examiner has determined that the material added by preliminary amendment to the written description and drawings is to be accorded benefit of a filing date earlier than the presentation of claims 63 through 67 because of an incorporation by reference appearing in a parent application. (See Paper Nos. 10 and 11.) Accordingly, we will consider the preliminary amendment as if part of the disclosure.

Atlantic Richfield Co., 208 F.3d 989, 1000, 54 USPQ2d 1227, 1235 (Fed. Cir. 2000), cert. denied, 531 U.S. 1183 (2001). However, one skilled in the art, reading the original disclosure, must be able to immediately discern the limitations now claimed. See Waldemar Link GmbH & Co. v. Osteonics Corp., 32 F.3d 556, 558, 31 USPQ2d 1855, 1857 (Fed. Cir. 1994) ("The fact finder must determine if one skilled in the art, reading the original specification, would immediately discern the limitation at issue in the parent.") Further, however, the question of written description support should not be confused with the question of what would have been obvious to the artisan. Whether one skilled in the art would find the instantly claimed invention obvious in view of the disclosure is not an issue in the "written description" inquiry. In re Barker, 559 F.2d 588, 593, 194 USPQ 470, 474 (CCPA 1977).

With these guidelines in mind, we find that appellants have pointed to material in the disclosure that is sufficient to meet the "written description" requirement of 35 U.S.C. § 112, first paragraph for the subject matter of instant claim 63. In particular, we find at least inherent support for the step (b) requirement of "sensing the presence of at least one activated cell from said number of memory cells that is erased to a state other than one of at least two data states." Step (5) of instant Figure 23 shows verification that "READ DATA = PROGRAM DATA" for all addressed cells. If there is no verification, the flowchart proceeds to step 6, which denotes applying a pulse of program voltage only to the addressed cells not verified. We find that the artisan would have immediately recognized that -- at least in the case identified by appellants in which

a cell is "programmed slightly" from the "erased" state -- there is necessarily a sensing that a cell is in an erased state. When the "read data" is not the same as the "program data," then the cell is in an erased state. In that event, the process flows to step (6) in Figure 23 for applying program voltage to cells not verified.³

We thus do not sustain the rejection under 35 U.S.C. § 112, first paragraph, for lack of written description support. To the extent the rejection may be based on the enablement requirement of the statute, neither do we sustain the rejection on that basis. The rejection does not consider and weigh the relevant factors that may lead to a conclusion of nonenablement. See In re Wands, 858 F.2d 731, 737, 8 USPQ2d 1400, 1404 (Fed. Cir. 1988).

³ Although drawings may provide "written description" support required by 35 U.S.C. § 112, first paragraph (see Vas-Cath, 935 F.2d at 1566, 19 USPQ2d at 1119), we refer to the drawings only for convenience. The algorithm is also described at pages 23 and 24 of the preliminary amendment.

Appeal No. 2001-1272
Application No. 09/056,398

CONCLUSION

The rejection of claims 63-67 under 35 U.S.C. § 112, first paragraph is reversed.

REVERSED

JOSEPH F. RUGGIERO
Administrative Patent Judge

Howard B. Blankenship
HOWARD B. BLANKENSHIP
Administrative Patent Judge

MAHSHID D. SAADAT
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Application No. 09/056,398

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**U.S. INTERNATIONAL TRADE COMMISSION,
INVESTIGATION NO. 337-TA-382**

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

PUBLIC INSPECTION

In the Matter of

CERTAIN FLASH MEMORY CIRCUITS)
AND PRODUCTS-CONTAINING SAME)

Investigation No. 337-TA-382

INITIAL DETERMINATION

Administrative Law Judge Sidney Harris

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OFFICE OF
UNFAIR IMPORT INVESTIGATIONS
U.S. INTERNATIONAL TRADE COMMISSION

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of)	
)	
CERTAIN FLASH MEMORY CIRCUITS)	Investigation No. 337-TA-382
AND PRODUCTS CONTAINING SAME)	
)	

INITIAL DETERMINATION
Administrative Law Judge Sidney Harris

Pursuant to the Notice of Investigation, 61 Fed. Reg. 7122-7123 (1996), this is the Administrative Law Judge's Initial Determination in the Matter of Certain Flash Memory Circuits and Products Containing Same, United States International Trade Commission Investigation No. 337-TA-382. 19 C.F.R. § 210.42(a).

The Administrative Law Judge hereby determines that a violation of section 337 of the Tariff Act of 1930, as amended, has been found in the importation and the sale within the United States after importation of certain flash memory circuits and products containing same by reason of infringement of claims 1, 2 and 4 of U.S. Letters Patent 5,418,752 and claim 27 of U.S. Letters Patent 5,172,338.

TABLE OF CONTENTS

	Page
Opinion	
I. Background.....	1
A. Procedural History.....	1
B. Technical Background.....	4
II. Importation and Sale.....	11
III. Claim Construction.....	12
A. General Law of Claim Construction.....	12
B. Construction of Claims 1, 2 and 4 of the '752 Patent.....	16
C. Construction of Claim 27 of the '338 Patent.....	49
IV. Validity.....	75
A. The '752 Patent.....	75
B. The '338 Patent.....	93
V. Infringement.....	103
A. General Law of Infringement.....	103
B. Claims 1, 2, and 4 of the '752 Patent Are Infringed.....	106
C. Claim 27 of the '338 Patent Is Infringed.....	115
VI. Domestic Industry.....	129

Findings of Fact

I. Background.....	142
II. Importation and Sale.....	152
III. Claim Construction.....	154
A. Construction of Claims 1, 2 and 4 of the '752 Patent.....	154
B. Construction of Claim 27 of the '338 Patent.....	162
IV. Validity.....	178

A.	The '752 Patent.....	178
B.	The '338 Patent.....	191
V.	Infringement.....	209
A.	The '752 Patent.....	209
B.	The '338 Patent.....	224
VI.	Domestic Industry.....	236
	Conclusions of Law.....	250
	Initial Determination and Order.....	251

C. Claim 27 of the '338 Patent

Claim 27 of the '338 patent is as follows:

In an array of addressable semiconductor electrically erasable and programmable memory (EEPROM) cells on an integrated circuit chip, the memory cell being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltage conditions for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions, a system for programming data to EEPROM cells including means for temporarily storing a chunk of data for programming a plurality of addressed cells, means for programming in parallel the stored chunk of data into the plurality of addressed cells, and means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data, wherein the improvement comprises:

means for inhibiting further programming of correctly verified cells among the plurality of addressed cells; and

means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly.

CX 2 at col. 26, lines 28-54.

Portions of the claim's lengthy preamble and the additional claim elements are at issue. According to Complainant a key feature of the claim 27 invention is allowing the programming of a chunk of cells in parallel, but treating each cell as if it were programmed individually for purposes of verification and inhibiting further programming of verified cells. Harari, Tr. 261-264 The preferred embodiment of claim 27 of the '338 patent describes a multi-state rather than a binary semiconductor device. The claim, however is not limited to the multi-state device. See e.g., CX 2 at col. 11, lines 56-61. Each of the portions of claim 27 which are in controversy will be

discussed below.

1. The Erase Electrode Element

The preamble of claim 27 recites as one of its elements "an erase electrode receptive to specific voltage conditions for reading, programming and erasing of data in the cell."

The term "erase electrode" is found in the '338 patent only in the claims.³⁴ CX 2. The term "electrode" is commonly understood in the semiconductor industry as a terminal to which an electrical signal is applied to perform some function. Pathak, Tr. 792, 918. An "erase electrode" is understood in the semiconductor industry as a terminal to which erase voltage conditions are applied to draw electrons off the floating gate. Pathak, Tr. 792. Thus, because the term "erase electrode" is not defined in the '338 patent as having anything other than its ordinary meaning, it is properly construed in the context of claim 27 as any terminal in a flash memory device to which erase voltage conditions are applied to draw electrons off the floating gate.

Respondents do not expressly contest this definition of "erase electrode" but argue that as used in the '338 patent, the term requires a separate structure for each cell which is dedicated specifically to drawing electrons off the floating gate. See, e.g., Respondents' Post-Hearing Br. at 20-21. Neither Complainant nor OUII adequately support this argument concerning the erase electrode.

Although the erase gate is used in the preferred embodiment as an erase electrode, various structures or terminals in a flash memory device can also

³⁴ See CPFF 257; SPFF 98.

function as an erase electrode as that term would be commonly understood, including the silicon substrate. Harari, Tr. 77-83. Indeed, the record shows that various companies (which are not parties to this investigation) have used the substrate instead of an erase gate as the terminal to which erase voltage conditions are applied to draw electrons off the floating gate during the erase operation. Harari, Tr. 77-83; CPX 25.

Respondents further argue that the silicon substrate cannot serve as an erase electrode in its devices because claim 27 requires that the erase electrode be "receptive to specific voltage conditions for reading, programming and erasing of data in the cell," and that [

[C]

] Respondents' Post-Hearing Br. at 21. As addressed below in the section on the infringement issue, it is found that at least certain of respondents devices satisfy this claim element.

2. The Increment/Decrement Element

The preamble of claim 27 imposes the limitation that the memory cell have "a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions."

All of the devices at issue in this investigation (Samsung and SanDisk devices) are binary devices.³⁵ Complainant argues that for a binary device,

³⁵ As discussed in the Background section of this Initial Determination, "multi-state" -- or "multi-level" -- devices are not currently in commercial use. See FF 30.

this element of claim 27 should be interpreted to cover a cell that achieves the programmed state by increment of the charge level with successive applications of programming voltage conditions, or a cell that achieves the erased state by decrement of the charge level with successive applications of erasing voltage conditions (or a cell that can perform both of these functions).

Respondents argue that the portion of claim 27 at issue includes two limitations: one requiring the successive application of voltage conditions to program (by putting charge on the floating gate) and the other requiring the successive application of voltage conditions to erase (by removing charge from the floating gate). They argue that "without the term 'or' this claim would merely recite counteracting applications of programming and erasing voltage conditions repetitively incrementing and decrementing charge without any net change in the charge level on the floating gate." Respondents' Post-Hearing Br. at 20-21.

OUII takes the position that claim 27 does not require successive applications of both programming voltage conditions and erasing voltage conditions.

Respondents argue that Complainant's interpretation of the word "or" allows for a broader construction of the patent claim than their interpretation. Citing the Federal Circuit's opinion in Athletic Alternatives, Inc. v. Prince Mfg., Inc., 73 F.3d 1573, 1581 (Fed. Cir. 1996), they argue that a court should adopt the narrower of two possible constructions, and that this element of claim 27 should be construed to cover only a device that achieves a specific memory state through successive applications of voltage, during programming and erasing. Respondents' Reply Br. at 10.

In Athletic Alternatives, the Federal Circuit highlighted the fact that patent claims perform the function of putting others on notice of the boundaries of the invention, and held, as follows:

Where there is an equal choice between a broader and a narrower meaning of a claim, and there is an enabling disclosure that indicates that the applicant is at least entitled to a claim having the narrower meaning, we consider the notice function of the claim to be best served by adopting the narrower meaning.

Id. at 1581.

However, claim 27 of the '338 patent does not present a case of an equal choice between two meanings. The simplest meaning of the claim element at issue is that one may use successive applications of programming voltage conditions or successive applications of erasing voltage conditions in order to practice the claimed invention. The word "or" in this instance serves its normal function of indicating the availability of an alternative or a choice.

Webster's at 1585.

Respondents would read an additional limitation into the claim by requiring that in every instance in which one sought to change the charge level of a cell one must make successive applications of programming or erasing voltage conditions. That additional limitation is not required by the language of the claim. Consequently, based on the plain language of the claim, there is not an equal choice to be made.

Furthermore, other evidence found in the specification and adduced at the hearing supports the broader construction of the claim. The increment/decrement element at issue corresponds to the programming algorithm illustrated in Fig. 15 (item 6), which is described in the text at col. 19, line 57 through col. 20, line 16, whereas the erasing algorithm is illustrated separately in Fig. 11 (items 1 and 2), which is described at col. 16, lines

18-25. With respect to both of these algorithms the charge on the floating gate is changed incrementally.

Thus, in the preferred embodiment disclosed in the specification, the patentees provided examples of incremental programming and of incremental erasing. See CX 2 at col. 18, lines 21-29. However, the fact that the preferred embodiment provides an example of each incremental operation does not mean that an additional limitation should be read into claim 27 that requires both incremental operations in all operations covered by the claim. See Loctite Corp. v. Ultraseal Ltd., 781 F.2d 861, 867 (Fed. Cir. 1985) ("Generally, particular limitations or embodiments appearing in the specification will not be read into the claims."); see also E.I. DuPont de Nemours & Co. v. Phillips Petroleum Co., 849 F.2d 1430, 1433 (Fed. Cir.), cert. denied, 488 U.S. 986 (1988) (prohibiting the reading of limitations from the specification into the claims "wholly apart from any need to interpret what the patentee meant by particular words or phrases in the claim").

The application of voltage conditions for programming and the application of voltage conditions for erasing are independent of each other. Harari, Tr. 1861, 1870. In both binary and multi-state devices, one may design for incremental programming and/or incremental erasing. However, programming and erasing are not part of the same operation. Harari, Tr. 1869; Pathak, Tr. 937.

Furthermore, in a multi-state device the reason for using incremental erasing is different from the reason for using incremental programming. In a multi-state device, different charge levels should correspond to different data. However, the consequences of over-erasing are endurance-related. The effect of over-erasing is not catastrophic to the performance of the device. Harari, Tr. 1870; Tutorial (Harari) Tr. 75-77; Guterman, Tr. 577-578.

Consequently, given the technical context in which the wording of claim 27 arose, it is proper that the claim be accorded the more ordinary, less complex meaning, such that one may use successive applications of either programming or erasing voltage conditions. It is not required that one use both program and erase incrementally in order to practice the claimed element.

3. The Temporary Storage Means

The preamble of claim 27 recites as one of its elements a "means for temporarily storing a chunk of data for programming a plurality of addressed cells." Complainant argues that in the context of this claim, the term "temporarily storing" would be understood by one of ordinary skill and should be interpreted to mean that the data for each cell is stored impermanently, but at least long enough to complete the programming of that cell. OUII argues that "temporarily storing" should be construed to mean storing as long as the individual cell in the chunk continues to receive the programming conditions. However, Respondents argue that "the term 'temporarily' must be construed to mean during the entire programming process for the entire chunk of data and not merely until a cell has been verified once." Respondents' Post-Hearing Br. at 22.

The evidence of record shows that in the context of the '338 patent, the term "temporarily storing" would be understood by one of ordinary skill to refer to a period of storage lasting at least as long as but not necessarily longer than the amount of time necessary to verify and terminate programming to the cell to which the stored data relates. After the programming of a cell is completed, the information used to program that cell is not used again. Harari, Tr. 248-249.

In claim 27 the patentees could have simply called for a means of

storing a chunk of data for programming.³⁶ However, they elected to add the word "temporarily" to the claim language. The term "temporarily" ordinarily means "for a brief period: during a limited time: briefly." Webster's at 2353. Thus, by adding the word "temporarily" the patentees have emphasized the brief nature of the data storage. That tends to support the claim interpretations proposed by Complainant and OUII, rather than Respondents. The brief nature of data storage is confirmed by reference to the specification and other evidence.

The means in question is disclosed in Figure 5, including block 190 (labeled "Read/Program Latches and Shift Registers"). Harari, Tr. 247-249; Thomas, Tr. 1509-1511; CX 2, at col. 19, line 27 through col. 20, line 36. It may be that in the preferred embodiment the data is stored in the latches until verification has occurred for the entire chunk of data stored therein, yet there is no express requirement to that effect. Thomas, Tr. 1510-1511; Pathak, Tr. 939. Moreover, after a particular cell to be programmed is verified, the data stored in the latch 190 serves no function for the cell that is already programmed, while the programming continues for the rest of the chunk. Harari, Tr. 247-249; Mehrotra, Tr. 329; Guterman, Tr. 587-588.

One of ordinary skill in the art knows that once programming and verification has taken place, the job is done for the stored data, and that "temporarily" in that case would mean just until the job is done. Pathak, Tr. 940-944. Thus, this element of claim 27 should not be construed so as to require storage of all data in a chunk until all cells to be programmed in accordance with the chunk of data have been programmed and verified. The data

³⁶ In the context of the '338 patent a "chunk" is "typically several bytes," and may be used to refer to the number of cells required to program the chunk. CX 2 at col. 19, lines 10-12.

need be stored only long enough for the programming and verification of the particular cell.

4. The Parallel Programming Means

The preamble of claim 27 of the '338 patent recites as one of its elements a "means for programming in parallel the stored chunk of data into the plurality of addressed cells." Complainant argues that in the context of claim 27, the phrase "programming in parallel" should be construed as referring to the function of simultaneously programming a plurality of cells, without reference to the manner of programming used. Respondents argue that the parallel programming means is limited to devices that program using a Hot Electron Injection ("HEI") programming process.³⁷ See Respondents' Post-Hearing Br. at 24.

Figure 14 of the '338 patent discloses certain structures with which the parallel programming function can be performed. CX 2 at col. 5, lines 40-41, col. 19, lines 27-41; Mehrotra, Tr. 330. In particular, Figure 14 shows an embodiment in which a Program Circuit with Inhibit, block 210, performs the parallel programming function, with the source multiplexer (or "mux") 107 and the drain mux 109 providing the data path. CX 2 at col. 19, lines 27-41; Mehrotra, Tr. 330-334. Thus, the parallel programming means should be construed to include these structures or their equivalents.

The cells in the preferred embodiment of the '338 patent are connected in a NOR architecture configuration. Pathak, Tr. 812-813. HEI programming is thus appropriate for use with the cells described in the preferred embodiment. Harari (Tutorial), Tr. 51-52; Mehrotra, Tr. 334-335. However, the language of claim 27 is silent on the cell structure and the corresponding programming

³⁷ HEI as well as the Fowler-Nordheim method of programming are discussed in the Technological Background section. See FF I 17-22.

method that must be used. Indeed, the '338 patent is not a patent on cell architecture such as NOR or NAND, and which programming method should be used with a particular cell structure. The patent merely recites the broad, general function of "programming in parallel" without specifying the programming method. One of ordinary skill in the art would know that parallel programming can be achieved in more than one way depending on the type of cell structure selected in a device. Furthermore, circuit designers are familiar with the various methods of programming cells depending upon their structures. Pathak, Tr. 944-946; Harari, Tr. 1861-1865. Thus, claim 27 should not be construed to require HEI programming.

In claim 27 of the '338 patent, "programming in parallel" means that programming takes place for more than one cell at a time, such that all cells selected for programming in accordance with a chunk of data receive programming conditions at the same time. See Harari, Tr. 76; Pathak, Tr. 807-808; CX 2 at col 19, lines 30-31 ("The EEPROM array 60 is addressed by N cells at a time.").

5. The Verifying Means *

The preamble of claim 27 recites as one of its elements "means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data."

The record evidence shows that the term "verifying" as it is used in claim 27 of the '338 patent normally would be understood by one of ordinary skill to refer to the process of determining whether the data in a memory cell matches the data that is targeted to be written into the cell.³¹ Guterman,

³¹ Mr. Thomas, Respondents' expert on whether Complainant SanDisk practices the '338 patent and on whether Samsung infringes the '338 patent, testified that the term "verify" is ordinarily used very loosely in the (continued...)

Tr. 489-490, 499. The '338 patent contains no contrary or inconsistent definition of the term.

However, Respondents point out that the claim language requires that the programmed data be verified "with" the chunk of stored data, and argue that claim 27 must read only on a device that verifies through the use of a comparator, as in the only structure disclosed in the '338 patent specification for verifying.

Questions are therefore raised as to whether claim 27 should be construed to require the use of a comparator, and whether a structure designed for use in a binary device can be equivalent to the structure disclosed in the '338 patent. These are especially pertinent questions because the Samsung and SanDisk devices at issue are binary devices and [[C]

] In a multi-state device, such as that described in the '338 patent's specification, a cell can be in one of several states. In performing the verification function, the first step is to determine the state of the cell to be verified (e.g., 0, 1, 2, 3). After determining the state the cell is in, the next step is to determine whether the cell is in the target state for that cell. If the cell is in the target state, the cell is verified; if not, further programming is required. Guterman, Tr. 490-493; CPX 46.

In a binary device, before programming can begin all cells must be in the erased state. Guterman, Tr. 493-495; CPX 48. Inasmuch as all cells start in the erased state, if the targeted state of a particular cell is the erased state, then the cell is in the targeted state before the programming cycle

"(...continued)
semiconductor industry to refer to the process of determining whether a cell is finished programming. Thomas, Tr. 1594-1595.

begins, and therefore no further action needs to be taken with respect to that cell. Harari, Tr. 264-265; Guterman, Tr. 493-495, 499-503; CPX 48. If the targeted state of a particular cell is the programmed state, and if the cell is not in the targeted state before the programming cycle begins, then programming pulses must be applied to bring the cell to its targeted state. Guterman, Tr. 493-495; CPX 48. For cells targeted to be in the programmed state, the cell is read after each programming pulse to verify whether the cell is in the programmed state (i.e., reads a "1"). Once the cell is sensed to be in the programmed state, further programming to that cell is terminated. Guterman, Tr. 493-495; CPX 48.

Figure 11-E of the '344 patent (which is incorporated by reference into the '338 patent) discloses circuitry that corresponds to the verify means in a multi-state implementation of the claim 27 invention. Figure 11-E depicts a multi-state implementation for a single cell in which the cell is able to hold one of four states. CX 2 at col. 4, lines 23-30; Guterman, Tr. 498-499; CX 3 (the '344 Patent); CPX 64. Figure 11-E discloses four sense amplifiers, one associated with each of the four states that the cell can hold. Each of the four sense amplifiers senses whether the current passing through the cell is greater or lesser than the reference current corresponding to the state associated with that sense amplifier. In the multi-state embodiment disclosed in Figure 11-E, once the sense amplifiers perform their sensing operation, the results are fed into the comparator disclosed in Figure 11-E, which determines whether the state of the cell matches the targeted state of the cell. Guterman, Tr. 499-503; CX 3, Fig. 11-E.

A binary embodiment equivalent to that disclosed in Figure 11-E of the '344 patent would not require all the circuitry disclosed for a multi-state implementation. Guterman, Tr. 499-503. In a binary device, it is unnecessary

to have more than one sense amplifier to perform the verification function of claim 27, since the only decision or verification that the device has to make is whether the cell is in the programmed state. Guterman, Tr. 499-503; Allen, Tr. 1173; CPX 64, CPX 66. For a binary device, it would be logical for a circuit designer to simplify the structure of Figure 11-E by eliminating three of the four sense amplifiers and the buffers and circuitry uniquely associated with those sense amplifiers, since they serve no function in a binary device and unnecessarily occupy surface area on the chip.³⁹ Furthermore, with a single sense amplifier, it is unnecessary to have a separate comparator circuit, since that comparator would merely replicate the function of the sense amplifier.⁴⁰ Guterman, Tr. 499-503; CPX 64, 66.

Consequently, the structure disclosed in Figure 11-E of the '344 patent could be reduced to a circuit with a single sense amplifier and no comparator for use in a binary device, and such a structure would be the structural equivalent of Figure 11-E. It could also be used to perform the function of verifying that addressed cells are in the correct state.

³⁹ Dr. Allen, Respondents' expert on the issue of patent validity, testified that a device that only verifies whether the cell is in the programmed state would satisfy the verify means of claim 27. As discussed further below in the section on patent validity, Dr. Allen testified that the "means for verifying" element of claim 27 is satisfied by the M293, a binary device that, like the SanDisk and Samsung flash memory devices, performs the verification function using a single sense amplifier (without a separate comparator circuit) to ascertain whether cells targeted to be programmed have reached the programmed state, while ignoring the cells targeted to remain in the erased state. See Allen, Tr. 1178-1180.

⁴⁰ The '344 patent expressly discloses that a single sense amplifier and a single reference level can be used to differentiate between conduction states "1" (which could indicated "programmed") and "0" (for "erased"). CX 3 at col. 26, lines 55-60. In fact, the '344 patent teaches that in a four-state storage device the comparison may be accomplished with four consecutive read cycles and only one sense amplifier, with a different reference applied at each cycle, if the additional time required for reading is not a concern. CX 3 at col. 25, line 64 through col. 26, line 17.

Figure 16 of the '338 patent discloses certain additional structures for performing the verification function in a multi-state device. In the circuit compare module 703 shown in the Figure, the read bits are compared bit by bit with corresponding program data bits, i.e., it is determined whether there is a match between the read and write data.⁴¹ This is performed by XOR (exclusive OR) gates such as 711, 713 and 715 shown in Fig. 16. The specification states that the number of such XOR gates used depends upon the number of binary bits encoded for each cell. The output of the XOR gates passes through a NOR gate 717 whenever all the bits are verified, and node 726 is taken high so that latch 721 is set in the verified state. Once latch 721 is set, the cell is inhibited from further programming during subsequent programming pulses that may be applied on the chunk. If, however, the read data does not match the write data, then latch 721 remains in its previous state.⁴² Mehrotra, Tr. 339-340; CX 2 at col. 20, lines 17-51.

The Figure 16 multi-state embodiment could be modified for a binary device by making some simplifications to the structures that would be obvious to an ordinary flash memory circuit designer. Mehrotra, Tr. 342; Pathak, Tr. 819-820.

In fact, the '338 patent contemplates an embodiment with only two states. The '338 patent expressly states in the context of discussing the verification function that "if each memory cell is to store K states, then at

⁴¹ In the preferred embodiment, "[C]ircuit 200 comprises N cell compare modules such as 701, 703, one for each of the N cells in the chunk." CX 2 at col 20, lines 18-20.

⁴² Figure 5 also provides a general identification of a "Compare Circuit", block 200, that performs the verify function in one embodiment of claim 27. The Program Circuit with Inhibit disclosed in block 210 of Figure 5 of the '338 Patent performs the function of inhibiting further programming by removing high voltage from the drain of the cell to be inhibited. Guterman, Tr. 508-510; Harari, Tr. 258, 267-269.

least $K - 1$, or preferably K reference levels need be provided. In one embodiment, the addressed cell is compared to the K reference cells using k sense amplifiers in parallel. This is preferable for the 2-state case because of speed" CX 2 at col. 11, lines 56-61. In other words, in the case of a two-state device, only a single reference level need be used for performing the verification function (e.g., where "0" equals the programmed state, the device only needs to determine whether the cell has reached the "0" state, and can ignore cells targeted to remain in the erased state).

It would be obvious to a circuit designer of ordinary skill to eliminate all but one of the XOR gates (711, 713, 715) in a binary device, since only one bit is being stored in the cell (i.e., "L" = 1). Mehrotra, 342-343; CPX 120; Pathak, Tr. 820-822; CPX 122. In a binary device, it would be obvious to a circuit designer of ordinary skill to change NOR gate 717 to a single inverter, since there would only be a single XOR gate, and therefore only a single input. Mehrotra, Tr. 342-345; CPX 120; Pathak, Tr. 820-822; CPX 122.

Furthermore, in implementing Figure 16 of the '338 patent in a binary device, the possible combinations of read (R) and write (W) are greatly reduced, as compared to a multi-state device, such that it is not necessary to implement the logic inherent in XOR (exclusive OR) gates and NOR gates to verify a cell.¹³ Thus, one would expect to make additional simplifications to the circuitry shown in Figure 16 by eliminating entirely the XOR gates and the NOR gate 717. Mehrotra, Tr. 345-351; CPX 120; Pathak, Tr. 819-829; CPX 122; CPX 127; CPX 128. It would be logical to simplify the verification and

¹³ There are only four logically possible states: $R=0$ and $W=0$; $R=0$ and $W=1$; $R=1$ and $W=0$; $R=1$ and $W=1$. For example, in the first scenario ($R=0$ and $W=0$), the data read from the memory is zero (erased) and the data desired to be written into the memory is also zero. Note also that the third scenario ($R=1$ and $W=0$) should not be possible because all cells are required to be in an erased state before programming starts. Mehrotra, Tr. 345-346.

inhibit circuitry disclosed in Figure 16 to consist merely of R (where R is the output of the sense amplifier) and the data latch 721, as shown in CPX 127. Mehrotra, Tr. 345-351; CPX 120; Pathak, Tr. 819-829; CPX 122; CPX 127; CPX 128. One familiar with the differences between multi-state cells and binary cells would simplify the verify and inhibit circuitry shown in Figure 16 to the circuitry shown in CPX 127, because such a simplification would reduce the size of the chip, reduce the logic, reduce costs, and give more efficient operation. Pathak, Tr. 829-829.

Based upon the language of claim 27, the specifications of the '338 and '344 patents, as well as extrinsic evidence adduced at the hearing, claim 27 is properly construed to cover a binary device that uses a single sense amplifier to verify whether a cell has reached its programmed state. Furthermore, it would not be logical to construe claim 27 to require the use of a comparator in a binary device. Accordingly, the claim 27 verification means should be interpreted to include the binary simplifications discussed above.

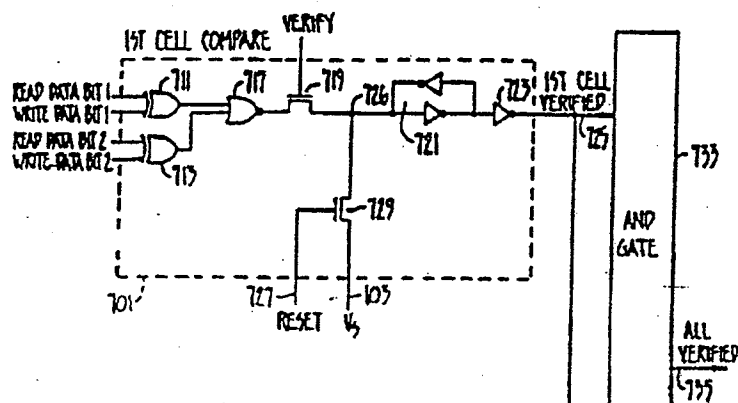
6. The Inhibiting Means

Claim 27 of the '338 patent recites as one of its elements "means for inhibiting further programming of correctly verified cells among the plurality of addressed cells."

Figure 16 of the '338 patent discloses one embodiment of the compare circuit used in the multi-state, preferred embodiment. Figure 16 also discloses circuitry that inhibits further programming of the memory cells. CX 2 at col. 20, line 17-18; Mehrotra, Tr. 340.

The pertinent circuitry is depicted in Figure 16 of the '338 as

follows:"



In the circuit shown in Figure 16, a latch 721 performs the function of inhibiting further programming to correctly verified cells. Mehrotra, Tr. 340-342. When a cell is correctly verified, the result is sent to latch 721, which is then set to the verified state. Mehrotra, Tr. 340; CX 2 at col. 20, lines 28-32. The specification mentions that at the end of a programming pulse all the latches are reset to the unverified state. Node 726 can only be reset by transistor 729 and not by node 717 after node 726 goes high. Mehrotra, Tr. 3. Once latch 721 is set in the verified state, the cell is inhibited from further programming during any subsequent programming pulses which may be applied.⁴⁵ Mehrotra, Tr. 340.

" The illustration, *supra*, like the illustration contained in Respondents' Reply brief, depicts the circuitry of one compare module contained in the preferred embodiment (compare module 701). Figure 16 and the text of the specification provide for "N compare modules such as 701, 703, one for each of the N cells in the chunk." CX 2 at col. 20, lines 18-20, Fig. 16.

⁴⁵ The '338 patent specification teaches that "[p]rogramming and verification are repeated until all the cells are correctly verified in FIG. 15(7)." CX 2 at col. 20, lines 14-16. Thus, each cell must be read to
(continued...)

Thus, latch 721 in Figure 16 is a "one-way latch." Latches are often referred to as "one-way" or "two way." One-way latches and two-way latches are often drawn in the same manner. Mehrotra, Tr. 372, 397. Yet, they function differently. A two-way latch freely switches back and forth between two states when different input values are applied. Thus, if the input to the latch is a 0, then the value saved in the latch becomes a 0. If a subsequent input is a 1, the latch then saves a 1. Allen, Tr. 1077. However, a one-way latch is said to move in only one direction. Thus, for example in Figure 16, when verification occurs and the latch is set to a 1, the latch does not go back to a zero during the overall cycle of iterations. See Allen Tr. 1078 (for the way a one-way latch works). Thus, a one-way latch like that used in Figure 16 of the '338 patent will not allow the detection of so-called "program disturb conditions" where, due to defects in a part, a cell goes back to an erased state before the entire chunk of data is verified. Nor will a one-way latch allow the detection of conditions in which a part fails and a cell is disturbed from an erase into a programmed state. Harari, Tr. 250-252; Mehrotra Tr. 374-378; CX 2. Furthermore, neither claim 27 of the '338 patent, nor the specification mentions the detection of program disturb conditions.⁴⁵

⁴⁵(...continued)
determine whether the read and write data for that cell match.

⁴⁶ Respondents state that Dr. Harari admitted that a device that verifies on an iteration basis would be within the scope of claim 27. See RPRFF 281 citing Harari, Tr. 270. Dr. Harari made the following statement during cross-examination in response to a hypothetical question:

Q. Well, let me ask you this. If -- if the Samsung device continued to verify, even if it was useless, would you say that it was outside the scope of this claim?

A. No, of course not.

Harari, Tr. 270.

(continued...)

CX 2.

With respect to Figure 16, the specification teaches that the output of the XOR gates passes through NOR gate 717 such that a "1" appears at the output of NOR gate 717 whenever all the bits are verified, otherwise a "0" appears there. When verification occurs (i.e. "[w]hen the control signal VERIFY is true"), "this result is latched to latch 721 such that the same result at the output of NOR gate 717 is also available at the cell compare module's output 725." CX 2 at col. 20, lines 25-32 (emphasis added). The output 725 is fed through an output line to the "program circuit with inhibit 210 of FIG. 5."⁴⁷ CX 2 at col. 20, lines 33-36.

The specification in describing the functions of latch 721 states that "[w]hen the control signal VERIFY is true, this result is latched to latch 721." It says nothing about setting latch 721 in case of a subsequent (or previous) control signal VERIFY that is not true. Thus, the specification does not provide that it will return to an unverified state during the program

"(...continued) ...

It is not clear what type of circuitry was assumed by the questioner or what type of circuitry Dr. Harari had in mind when he responded. It is significant that Dr. Harari was asked about a device that somehow continued to "verify, even though it was useless," not about a circuit that continued to apply programming conditions. Claim 27 requires an inhibition against further programming, not further, useless verification. The hypothetical circuit in question did not exclude the fact that it would have an operational program inhibit as required by claim 27.

⁴⁷ The program circuit is the circuit that removes voltage from a cell so that further programming (or over-programming) cannot take place. However, as described in the specification, the program circuit depends upon the data latched by latch 721. Although latch 721 is physically contained within the compare module in the preferred embodiment, the results of the comparison of read and write data are latched to latch 721. Latch 721 does not perform that comparison. It plays a role in making sure that correct output is available from the compare module for input to the program circuit.

and verification of a chunk of data." Indeed, since latch 721 is a one-way latch, once the latch is set, the stored data cannot be affected by the output of NOR gate 717. Mehrotra, Tr. 340-341.

The preferred embodiment of the '338 patent is a multi-state device. If latch 721 were not a one-way latch, there would be catastrophic failure of the multi-state device. See McGreivy, Tr. at 1697-1701, 1797-1799; CX 2 at col. 19, lines 4-26. The specification provides that in order to change the setting of latch 721:

At power-up or at the end of program/verify of a chunk of data, all cell compare module's outputs such as 725, 727 are reset to the "not verified" state of "0". This is achieved by pulling the node 726 to V_{ss} (0 V) by means of the RESET signal in line 727 to a transistor 729.

CX 2, col. 20, lines 46-51.

Thus, the specification teaches that latch 721 must be reset at power up, as well as at the end of each program/verify of a chunk of data. The '338 patent also teaches that before any programming occurs, a read operation must

" Respondents' expert, Dr. Allen, testified at the hearing that latch 721 is a two-way latch. His opinion appears to be based in part on an incorrect reading of the specification text. Referring to column 20, starting at line 28, he testified as follows:

So we're pointing out that indeed in the language of the specification, the specification calls for on any given iteration within the overall cycle, whatever value is read out on the NOR gate 717 is to be brought over here to the node 725. The only way for that to happen consistently on every iteration as indicated by the language I just read, is for latch 721 to be able to go back and forth. That is to be a two-way latch.

Allen, Tr. 1086 (emphasis added).

However, the specification does not state that whatever value is read out on NOR gate 717 is to be brought over to node 725. As discussed, *supra*, the specification states in column 20 that the output of NOR gate 717 is available at the cell compare module's output 725 only when the control signal VERIFY is true.

be performed to verify that the read data and the write data match. Thus, if latch 721 were a two-way latch, before the commencement of programming a cell would be read and if found not to be in the correct state, latch 721 would flip back to the not verified state in response to the output of NOR gate 717. A reset operation such as that disclosed in the specification would not be required. Mehrotra, Tr. 399-400. Instead, the specification shows that latch 721 can only be reset by the effect of transistor 729. See Mehrotra, Tr. 342. The specification demonstrates that latch 721, once set to the verified state, remains in the verified state during the entire program/verify of a chunk of data. Then, latch 721 is returned to the "not-verified" state by a reset operation in which node 726 is pulled down, as one would expect in the case of a one-way latch."⁹ See Mehrotra, Tr. 400; Allen, Tr. 1079, 1086.

In addition to the disclosure of Figure 16, including latch 721, Figure 5 of the '338 patent contains a block 210 entitled "Program Circuit with Inhibit." This block provides no detail regarding the specific circuitry that actually inhibits further programming. CX 2; Guterman, Tr. 508-510. Figure 17 shows "one embodiment of the program circuit with inhibit 210 of Fig. 5 in more detail." CX 2 at col. lines 52-53. The one embodiment shown in Figure 17 is relevant to the Hot Electron Injection programming method used in the preferred embodiment. The circuitry in Figure 17 is for removing voltage from the drain of a cell to inhibit further programming. CX 2 at col. 20, line 52 through col. 21, line 8; Mehrotra, Tr. 352-353; Guterman, Tr. 511-513.

Respondents argue that the means for inhibiting further programming of

⁹ In order to pull down latch 721, one would have to design the circuit shown in Figure 16 to have transistors of the proper size. Allen, Tr. 1079; Mehrotra, Tr. 409. The '338 patent does not indicate the size of the transistors involved in Figure 16. Nonetheless, one of ordinary skill would know how to size the transistors shown in Figure 16 relative to the size of NOR gate 717 so as to achieve a one-way latch. CX 2; Mehrotra Tr. 404-409.

correctly verified cells among the plurality of addressed cells is the program circuit disclosed in Figure 17 of the '338 patent. Respondents' argument with respect to the inhibit means is linked to their argument that HEI programming and a cell that uses such programming must be used in the claimed invention. See Respondents' Post-Hearing Br. at 26-27, RPFF 463-465. This argument has been rejected above in the discussion of the parallel programming means. Furthermore, although the circuitry disclosed in Figure 17 is part of one way of implementing the claimed invention, it depends upon circuitry that is actually located with the "compare modules," e.g., latch 721 and compare circuit module output 725.

To one skilled in the art, one way of implementing the inhibit means is to combine certain disclosures in Figures 16 and 5, in particular block 190 of Figure 5, which is entitled "Read/Program Latches and Shift Register." The temporary storage latch disclosed in block 190 of Figure 5 can also serve as the inhibit latch 721 of Figure 16 of the '338 patent. Mehrotra, Tr. 349-351; CPX 120; CX 2, Fig. 16; Pathak, Tr. 835-839; CPX 57C-58C; CPX 124-125. A flash memory designer of ordinary skill would seek to combine the functions of the temporary storage latch and the verify inhibit latch in a single structure in order to save transistors, thereby reducing the surface area of the chip. Pathak, Tr. 839-840.

Consequently, the inhibit means should be interpreted to include a one-way latch 721 or its equivalent.

7. The Final Means Plus Function Element

Claim 27 recites as its final element "means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly."

Complainant argues that this element refers to an iterative process in which the cells are repeatedly verified, utilizing additional programming pulses until all of the addressed cells have been verified. The claimed uniqueness of complainants invention is that the successive programming pulses are applied to only those cells which have not yet been correctly verified (i.e. have not reached their desired state at which point all further programming to already verified cells is permanently inhibited through the remainder of the program cycle).⁵⁰

Respondents argue, however, that Complainant would interpret claim 27 to place an additional "permanently inhibit" limitation on the programming algorithm of the '338 patent. According to Respondents, the '338 device does not permanently inhibit programming of cells that are erroneously verified as correctly programmed. See, e.g., Respondents' Post-Hearing Br. at 14; Respondents' Reply Br. at 12-16.

Figure 16 of the '338 patent discloses structures that correspond to the final means-plus-function element of claim 27 in a multi-state implementation. Those structures include the one-way latch 721, the outputs such as output 725, as well as AND gate 733 whose single output 735 is used to signal the controller in the preferred embodiment that all cells in the chunk of data have been correctly verified. Mehrotra, Tr. 341; CX 2 at col. 20, lines 18-51. Accordingly, the final element of claim 27 should be construed to include these structures or their equivalents.

The parties disagree as to the plain meaning of the patent claim. In particular, there is disagreement as to the effect of the final phrase "until

⁵⁰ OUII agrees with Complainant that "claim 27 is limited to devices which inhibit programming of correctly verified cells for the period of time until all cells are verified correctly." OUII argues that this feature is enabled by latch 721 in Figure 16. OUII Reply Br. at 17 & n.21.

all the plurality of addressed cells are verified correctly." Given the lack of punctuation in the text of the claim and the ordinary meaning of the words contained in that phrase, it appears that the condition specified therein applies to the entirety of the claim language preceding it within the final element, i.e., to both (1) further programming and verifying and (2) inhibiting programming of correctly verified cells. That appears to be the same position taken by Respondents, at least as regards the grammatical function of the final "until" phrase contained in the claim element. See Respondents' Post-Hearing Br. at 9-10; Respondents' Post-Hearing Reply Br. at 12.

The Administrative Law Judge reads this final phrase to refer to the fact that the verification and programming process continues until the entire chunk of data is programmed. However, the fact that the final phrase modifies the entire claim element does not require the meaning for the final element proposed by Respondents. Although the final claim element requires further programming until all cells are correctly verified, that does not mean that once a cell is correctly verified that the device must then verify it again and, more significantly, if found no longer to be in the target state that the inhibition against further programming must be removed and the cell must be reprogrammed. Such a limitation is not contained in claim 27, and to construe claim 27 in that manner would ignore the express requirement that programming be inhibited from cells once correctly verified. To construe claim 27 to require that cells which have been correctly verified must be subject to further programming would also be inconsistent with the proper construction of the previous claim element (the inhibiting means), which as discussed above requires a one-way latch like latch 721 in the preferred embodiment or its equivalent.

Furthermore, the description of the means described in the '338 patent specification requires that the programming of each cell be permanently inhibited upon verification.⁵¹ For example, the specification provides in part: "[a]s soon as the programmed state is verified correctly, programming stops." CX 2 at col 18, lines 24-25. The patent provides further that "parallel programming is implemented by a selective programming circuit which disables programming of those cells in the chunk that have already been verified correctly." CX 2 at col. 19, lines 13-16. Finally, the patent also provides that "it is preferable to apply programming voltages in repetitive short pulse with a read operation occurring after each pulse to determine when it has been programmed to the desired threshold voltage level, at which time the programming terminates." CX 2 at col. 9, lines 13-18. Each of the passages clearly indicates that the '338 patent will not apply an additional programming pulse to a cell after it has been verified. See Mehrotra, Tr. 253-254; McGreivy, Tr. 1693-1696.

⁵¹ Respondents argue that Figure 15 shows that individual cells may be either programmed or inhibited in any individual pulse. See Respondents' Post-Hearing Br. at 4-5; Respondents' Reply Br. at 12; Thomas, Tr. 1510-1511. Figure 15 is a block diagram that depicts an on-chip program algorithm according to the claimed invention. CX 2 at col 5, lines 42-43, Fig. 5. The algorithm is discussed in the text at col. 19, line 57 through col. 29, line 16. The block at Fig. 15(5) is labeled "Verify Read Data = Program Data For All Addressed Cells." If the answer is "No" the diagram indicates in block 6 that a pulse of program voltage is to be applied only to addressed cells not verified. Respondents interpret this diagram to indicate that each cell must be given an additional programming pulse if upon any verification pulse the cell is found not to be verified correctly. However, Figure 15 cannot be read in isolation. It is given clarity by Figure 16, whose latch 721 operates throughout the programming of a chunk of data to identify a cell as correctly verified once it has reached a programmed state. Thus, a cell once correctly verified will be read as such each time the program algorithm reaches the stage depicted in Fig. 15(5), and in accordance with block (6) such a cell will not receive a further program pulse. Such a cell is permanently inhibited from further programming while the remainder of the chunk of data is programmed.

The distinction between conditional inhibition and termination is an important one. As Dr. McGreivy explained, failure to terminate will, over time, overstress a binary device and make a multi-state device malfunction. McGreivy, Tr. 1697-1708, 1793-1813. This point is addressed in the text of the '338 patent, as follows:

In the prior art EEPROM devices, after each programming step, the state attained in the cell under programming is read and sent back to the controller 140 or the CPU 160 for verification with the desired state. This scheme places a heavy penalty on speed especially in view of the serial link.

In the present invention, the program verification is optimized by programming a chunk (typically several bytes) of cells in parallel followed by verifying in parallel on chip. The parallel programming is implemented by a selective programming circuit which disables programming of those cells in the chunk whose states have already been verified correctly. This feature is essential in a multi-state implementation, because some cells will reach their desired state earlier than others, and will continue pass [sic] [past] the desired state if not stopped. After the whole chunk of cells have been verified correctly, logic on chip communicates this fact to the controller, whereby programming of the next chunk of cells may commence. In this way, in between each programming step data does not need to be shuttled between the EEPROM chip and the controller, and program verification speed is greatly enhanced.

CX 2 at col. 19, lines 4-26.

Based upon the plain language of claim 27, the discussion of this issue in the specification, and the disclosure of the one-way latch 721, claim 27 is properly construed to include the limitation of termination or permanent inhibit of programming once a cell has been correctly verified.

B. The '338 Patent

Samsung's on-sale bar, anticipation and obviousness affirmative defenses against claim 27 of the '338 patent depend on its argument that the claim covers EEPROM devices that inhibit the programming of correctly verified cells for only one iteration. As discussed in detail above, Samsung's proposed construction of claim 27 has not been adopted. It has been found as a matter of law that claim 27 requires permanent inhibition of further programming pulses to a cell that has been verified during the programming of a chunk of data. Consequently, Samsung has not in connection with its affirmative defenses established by clear and convincing evidence that claim 27 of the '338 patent is invalid.

1. On-Sale Bar

Respondents argue that a television tuner manufactured by SGS Thomson, and identified as the M293 device, anticipates claim 27 of the '338 patent, and acts as an on-sale bar under 35 U.S.C. § 102(b), thereby making claim 27 invalid.⁶⁷ Complainant and OUII take the position that Respondents have not shown by clear and convincing evidence that the claim is invalid.

In order to establish an on-sale bar, the Samsung Respondents have the burden of demonstrating by clear and convincing evidence that each element of claim 27 is embodied in the M293 device. See Ferag AG v. Quipp, Inc., 45 F.3d

⁶⁷(...continued)

'752 is not deficient in that regard. However, Respondents did not raise this issue in their briefs, and the issue is therefore abandoned. See OUII's Reply Br. at 14 n.18.

⁶⁸ Under 35 U.S.C. § 102(b), "[a] person shall be entitled to a patent unless the invention was . . . in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States."

1562, 1566 (Fed. Cir.), cert. denied, 116 S.Ct. 71 (1995).⁹ However, the evidence of record shows that the M293 device does not perform the claimed function of permanently inhibiting the programming of correctly verified cells "until all the plurality of addressed cells are verified correctly" and therefore cannot act as an "on-sale bar" under 35 U.S.C. § 102(b).

Exemplars of the M293 device were the subject of testing performed during the course of this investigation in order to determine whether the device embodies each of the elements of claim 27 of the '338 patent. Particular emphasis was placed on the device's ability to inhibit programming pulses to correctly verified cells. The testing performed on behalf of Respondents is reflected in the TAEUS Report (RX 180C). SanDisk performed its in-house tests and submitted a Report (CX 199). Testing that was agreed to by both SanDisk and Samsung is reflected in the Chipworks Report (CX 204). Although TAEUS, SanDisk and Chipworks used different testing protocols and conditions, each demonstrated that the M293 device is not capable of permanently inhibiting programming of correctly verified cells as required by claim 27 of the '338 patent.

The TAEUS Report submitted by Samsung shows that the circuitry of the M293 device lacks any structure capable of permanently inhibiting the correctly verified cells from further programming. FF IV 101-102. The M293 test Report submitted by SanDisk, as testified to by Mr. Mehrotra of SanDisk, establishes that the M293 device does not perform the function of permanently inhibiting the programming of verified cells until all the plurality of addressed cells are verified correctly, and does not have the structure to do so. FF IV 98-102. Furthermore, the Chipworks Report also shows that the M293

⁹ SanDisk does not dispute that the SGS device was on sale in the United States more than one year before the '338 patent application was filed.

device does not permanently inhibit the correctly verified cells from further programming, or contain circuitry necessary to meet that claim limitation. FF IV 123, 133, 140.

The most significant differences between the M293 device and the structure and the function required by claim 27 are due to the fact that the verification and inhibiting circuitry of the M293 does not include a "one-way" latch that terminates the programming of a cell upon verification. See FF IV 102. Consequently, unlike the invention claimed in the '338 patent, the M293 device only inhibits verified cells on a temporary or conditional basis. FF IV 101.

For example, if a particular bit verifies as programmed after the third programming pulse in the M293 device, it will be inhibited from programming on the fourth pulse. However, since each cell is reverified after each subsequent programming pulse, if the cell should then fail the verification step following the seventh programming operation (e.g., because it was a borderline pass or because an error occurred in the read/verify step), the cell will then receive an additional programming charge during the eighth programming pulse. Gross, Tr. 1453-1454. Thus, the M293 device does not inhibit "programming of correctly verified cells until all the plurality of addressed cells are verified correctly." See FF IV 99.

In addition to proposing a different interpretation for claim 27, Samsung argues that the M293 performs the claimed function of terminating the programming of verified cells because in "normal operation" the device will not apply an additional programming pulse to a cell that has been already verified.

Samsung contends that the additional programming pulses issued to already verified cells during Chipworks testing of the M293 device is

attributable solely to variations in the input voltage and the capacitive loading of the equipment. However, Chipworks concluded that this could not be the case for at least certain of the wave forms generated during testing. See FF IV 145-152.

Furthermore, the purpose of the permanent inhibit function of the '338 patent is to prevent the application of a programming pulse to a cell in those situations where the device experiences a misread or false verify.⁷⁰ See McGreivy, Tr. 1697-1708; section on claim construction. Thus, Samsung's argument concerning supposedly normal operations of the M293 does not show that the device contains all the elements of claim 27 of the '338 patent.

Therefore, for the reasons stated above, sales of the SGS M293 device did not act as an on-sale bar to the patentability of claim 27 of the '338 patent.

2. Anticipation (the Torelli Article)

Respondents argue that an article by Guido Torelli, et al., entitled "An Improved Method for Programming a Word-Erasable EEPROM" (the "Torelli Article") ((RX 71) anticipates claim 27 of the '338 patent, thereby making the claim invalid.⁷¹ See FF IV 153. The Torelli Article describes the operation and characteristics of the M293 device. FF IV 154. Complainant and OUII take

⁷⁰ Such occurrences take place under normal conditions without the presence of any testing equipment. See Allen, Tr. 1177.

⁷¹ Respondents' arguments concerning alleged anticipation by the Torelli Article are based on Section 102(b) of the Patent Act, which provides that a person is not entitled to a patent if:

the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States

the position that Respondents have not shown by clear and convincing evidence that the claim is invalid."⁷²

In order for the Torelli Article to anticipate claim 27 of the '338 patent, it must be proven by clear and convincing evidence that "all of the elements and limitations of the claim are found within [this] single prior art reference." Scripps Clinic & Research Found. v. Genentech, Inc., 927 F.2d 1565, 1577 (Fed. Cir. 1991)."⁷³

As in the case of the M293 device, the Torelli Article does not disclose the function of permanently inhibiting the programming of verified cells. FF IV 154-160. Figure 4 of the Torelli Article and its associated text show that all the cells being programmed are "read/verified" between each and every programming pulse. FF IV 157-158."⁷⁴ At trial, all the witnesses uniformly agreed that the M293 device discussed in the Torelli Article does not perform the claimed function of permanently inhibiting the programming of correctly verified cells. FF IV 154-155, 99-102, 151-160. Indeed, there is no structure disclosed or suggested in the Torelli Article, such as a one-way

⁷² Prior to the hearing, the Administrative Law Judge was informed that Complainant and Respondents sought reexamination of the '338 patent in light of the Torelli Article, and SGS brochures and technical notes. The Administrative Law Judge did not believe it suitable to suspend this investigation based on the particular circumstances existing in this case, including: the fact that the hearing was imminent and the parties had virtually completed preparations for the hearing; the lack of detailed statements from the PTO concerning the effect of the Torelli Article or other references on the '338 patent; and the likelihood of a substantial period of time before a definitive decision would be made by the PTO.

⁷³ It was not disputed that the Torelli Article was published early enough so that it could be cited against the '338 patent under section 102(b).

⁷⁴ In fact, the related M293 device will apply a programming pulse to a cell whenever that cell is read by the device to be in the unprogrammed state regardless of whether it was verified and inhibited during the application of a previous programming pulse. FF IV 154-155, 159-160, 165.

latch, to track whether a cell was verified/inhibited during the application of a previous pulse so as to disable any further programming of that cell. FF IV 159-160.

In addition to the dispositive absence of the termination function, it has not been established that the Torelli Article contains sufficient disclosures of structures required to perform other functions required by claim 27.

The Torelli Article does not disclose any structure for temporarily storing a chunk of data for programming a plurality of addressed cells. FF IV 161. Although one may infer that there is a location for temporarily storing data, it is not clear from the article whether temporarily stored data is to be stored on or off chip. FF IV 162; McGreivy, Tr. 1759-1763.

The Torelli Article does not disclose any structure for verifying the programmed data in each of the plurality of addressed cells with a chunk of stored data. Without further disclosure in the article, one of ordinary skill in the art would not know the type of structure to use for the verification function. FF IV 166.

Finally, the Torelli Article does not disclose any structure for further programming and verifying in parallel the plurality of addressed cells and inhibiting the programming of verified cells until all the plurality of addressed cells are verified. The article does not disclose the type of verification and program inhibit functions required by claim 27 of the '338 patent, let alone a means for continuing such functions until all the plurality of addressed cells are verified. See FF IV 165, 166.

Aside from the failure by the Torelli Article to disclose these elements required by claim 27 of the '338 patent, the insufficiency of disclosure would also deny an individual of ordinary skill the ability to build the device

disclosed in claim 27 of the '338 patent. FF IV 159-166. Consequently, the lack of enablement by the Torelli Article prevents it from anticipating claim 27 of the '338 patent, independently of its failure to disclose the program inhibit element. See Akzo N.V. v. United States Int'l Trade Comm'n, 808 F.2d 1471, 1479 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987) (in order to anticipate a claimed invention, a prior art reference must be enabling, thus placing the allegedly disclosed matter in the possession of the public).

Given the total absence in the Torelli Article of key structures and limitations required by the patent claim, it has not been shown by clear and convincing evidence that the Torelli Article anticipates claim 27 of the '338 patent.

3. Obviousness

Respondents argue that the Torelli article and the devices and product literature (SGS data books and technical notes) based on it render the claimed invention of the '338 patent obvious under 35 U.S.C. § 103, and therefore invalid.⁷⁵ Complainant and OUII take the position that Respondents have not shown by clear and convincing evidence that the '338 patent is invalid.

In order to prove obviousness, it must be demonstrated by clear and convincing evidence that the invention of claim 27 would have been obvious in light of the combined teachings of items of prior art relied on by Respondents. See Graham v. John Deere, 383 U.S. at 37; Jones, 727 F.2d 1524, 1530-32 (Fed. Cir. 1984); Litton, 97 F.3d at 1566 (section 103 obviousness analysis requires a determination of the scope and content of the prior art, the differences between the prior art references and the claimed invention and the secondary indicia of nonobviousness). In addition, it must be shown that

⁷⁵ Section 103 of the Patent Act is quoted above in the portion of this section addressing the '752 patent.

one of ordinary skill would have known to combine these items. See Uniroval, 837 F.2d at 1050-1051.⁷⁶ As discussed below, the requisite showing has not been made to find claim 27 of the '338 patent obvious in view of the prior art.

Neither the Torelli Article, nor the SGS data books, nor SGS technical notes include any disclosure or teaching relating to the concept of permanently inhibiting the programming of verified cells, an essential function of claim 27. FF IV 175-189. Furthermore, Samsung introduced no evidence at trial to show that the permanent inhibition of programming of verified cells would have been obvious to an individual of ordinary skill. FF IV 191. Nor did Samsung offer any testimony to suggest that one would know to combine the cited prior art. FF IV 192.

In fact, Samsung has argued against obviousness by taking the position that the function of permanently inhibiting the programming of correctly verified cells would be irrelevant or meaningless to the operation of binary devices. Thus, Samsung has conceded that an individual of ordinary skill would not recognize the possibility that the endurance and operation of a binary EEprom device could be improved by terminating the programming of correctly verified cells. See also FF IV 198, 199.

There is nothing in the prior art relied on by Samsung to indicate that the programming of a cell should be stopped or terminated upon verification. FF IV 175-189. In fact, the Torelli Article, SGS data books and SGS technical notes suggest the opposite. These documents suggest that all the cells being programmed should be verified after each programming pulse. At most, they

⁷⁶ An individual of ordinary skill in the art of flash memory has at least a bachelor's degree in a field such as electrical or computer engineering (or experience equivalent thereto) and at least a few years of work experience with EEproms. FF IV 167-172.

teach that the inhibition of further programming pulses is a conditional event that must occur on a pulse-by-pulse basis. FF IV 155-158. Thus, if the "read" conditions on any given cell changes after a cell has been "verified" (*i.e.*, the device correctly or incorrectly reads that the cell is no longer in the "written" state), the respective disclosed devices apply an additional programming pulse(s) to the previously verified cell. FF IV 154, 100. Such a result is contrary to the requirement of claim 27 that the programming of a verified cell be inhibited or disabled until all the addressed cells have been verified.

Furthermore, it was undisputed at trial that the concept of "permanently inhibiting" or "terminating" the programming of verified cells was not obvious to an individual of ordinary skill in 1989. See FF IV 198-226. The non-obviousness of the permanent inhibit feature is demonstrated by the fact that Toshiba, the original designer of the NAND architecture, did not include a permanent inhibit feature in its original 4Mbit flash memory product despite the fact that it is beneficial to the NAND device. FF IV 199, 226.

Consequently, none of the prior art cited by Samsung can individually or in combination invalidate claim 27 of the '338 patent.

The validity of the '338 patent, including claim 27, is further supported by secondary indicia of validity. The '338 patent has been and will be crucial to SanDisk's success in the mass storage flash memory market. FF IV 200. As of 1994, SanDisk was the worldwide leader in the mass storage flash memory with approximately a 40% market share. FF IV 203. Furthermore, Intel, the world's largest commodity flash memory producer, has entered into a licensing agreement for all of SanDisk's patents, including the '752 and '338 patents. FF IV 201.

The Administrative Law Judge finds that it has not been shown by clear and convincing evidence that claim 27 of the '338 patent is invalid due to obviousness.

C. Claim 27 of the '338 Patent Is Infringed

Complainant SanDisk takes the position that Samsung's devices practice each of the elements of claim 27, including the seven disputed elements covered in the section of this Initial Determination on claim construction, and that therefore Samsung infringes claim 27 literally or, in the alternative, under the doctrine of equivalents.

The Samsung respondents take the position that their devices do not practice at least six of the disputed claim elements, and that therefore their devices do not infringe claim 27 either literally or under the doctrine of equivalents. Respondents' Post-Hearing Br. at 17.

OUII takes that position that the Samsung devices do not practice all of the disputed elements of claim 27, and that therefore the devices are not infringing.

Samsung's Flash EEPROM products are binary devices. As discussed above in the section on claim construction, although the preferred embodiment of the '338 patent is a multi-state device, the specification states that the claimed invention may be applied to a binary device. Indeed, claim 27 reads on a binary device. However, Samsung argues that because of prosecution history estoppel, a binary device cannot be found to infringe claim 27. SanDisk and OUII oppose Samsung on this point.

Before examining each of the individual elements of claim 27, the question of prosecution history estoppel is addressed as a threshold matter.

Samsung argues that during the prosecution of the '338 patent, SanDisk distinguished claim 27 over U.S. Patent No. 4,460,982 to Gee et al. on the basis that the '982 Gee patent would work only for binary memory cells, not multistate cells covered by the '338 patent, and further that SanDisk is estopped from now asserting that binary devices infringe the asserted claims

under the doctrine of equivalents.

In order to distinguish claim 27 of the '338 patent over the prior art, particularly Gee et al., the applicants' agent represented, as follows:

Claim 27-28 has [sic] been amended to recite inhibiting of further programming of correctly verified cells rather than selective programming of unverified cells.

Gee et al. disclose a programming system operating in parallel on 8 bits of addressed cells. If bits 2, 5 and 7 are to be programmed to the "0" state, programming pulses will be applied to all three cells as long as one of these cells are not verified correctly. This scheme does not work for memory cells having more than two states since some cells will reached [sic] their desired state earlier than others and will continue to pass [sic] the desired state if not stopped.

Thus, Giebel and Gee et al., individually or in combination do not teach or suggest a programming system with means for inhibiting further programming of correctly verified cells among the plurality of addressed cells. It is believed amended claims 27-28 along with amended claim 33 are allowable.

CX 8 ('338 Prosecution History) at SD008951 (emphasis added).

The statements quoted above, and relied on by Respondents (see RPFF 373), say nothing about binary devices. The applicants, through their agent, indicated to the Examiner that their invention, as claimed in claims 27-28 and 33, is suitable for multistate devices because of its ability to inhibit further programming of correctly verified cells, whereas Gee et al. is unsuitable for multistate devices. However, the statements made to the Examiner do not preclude the claim from covering binary devices. These statements pointing out the advantages of the claimed invention with respect to multistate devices do not indicate that the claimed invention and that of Gee et al. operate in the same manner with respect to binary devices. Indeed, the inhibiting of further programming of verified cells occurs regardless of whether the invention of claim 27 is used in a binary device or a multistate

device. As discussed above in connection with claim construction, it is also useful to prevent unnecessary programming in both binary and multistate devices.

Therefore, the Administrative Law Judge finds that prosecution history estoppel does not apply in the case of the '338 patent to prevent claim 27 from covering binary devices such as Samsung's flash EEPROM products.

Consequently, Samsung's devices and the disputed elements of claim 27 of the '338 patent are discussed below. For the purposes of this infringement analysis, all of Samsung's products are addressed together." See FF V 119, 136.

1. Erase Electrode Element

[[C]] in Samsung's flash memory devices constitutes an erase electrode as that term is used in claim 27 of the '338 patent. See FF V 123. As noted above, "erase electrode" is properly defined in the context of claim 27 as a terminal to which erase voltage conditions are applied to draw electrons off the floating gate. See, supra, at 51: [

[C]

] FF V 125-131. This functionality squarely falls within the properly interpreted scope of the term "erase electrode."

Samsung attempts to avoid a finding of infringement by reading

" The Samsung devices are not addressed as having "old" or "new" designs for the purposes of an infringement analysis under claim 27 of the '338 patent. Samsung's redesign was directed at the multi-block erase feature of its devices, which is not the subject matter of the '338 patent.

additional limitations into this element (e.g., that there must be a separate erase electrode for each cell, or that it must be "physically distinct" from any other structure in the device). However, there is no language in the patent or the file history that would require the imposition of these limitations or otherwise vary the ordinary meaning of the term. Thus, the erase electrode limitation must be properly interpreted (as both SanDisk and OUII have argued) in accordance with its ordinary meaning and without Samsung's additional proposed limitations. Applying this interpretation, Samsung's flash memory devices clearly satisfy the "erase electrode" element.

The Administrative Law Judge finds that given its proper interpretation, the term "erase electrode" is broad enough to encompass Samsung's devices under the standards of literal infringement. However, SanDisk and Samsung have raised the issue of the doctrine of equivalents with respect to this claim element.

As an alternative to literal infringement, Samsung's devices would satisfy this claim limitation under the doctrine of equivalents. Samsung argues that its devices do not satisfy this element under the doctrine of equivalents because there are differences between [[C]] and the erase gate disclosed in the preferred embodiment. See, e.g., Respondents' Post-Hearing Br. at 22.

The relevant inquiry under the doctrine of equivalents is not merely whether there are structural differences between the accused devices and the preferred embodiment, but whether the differences between the claimed erase electrode and the Samsung structure are substantial (e.g., whether one of ordinary skill would have known of the interchangeability of [[C]] and the erase electrode of the preferred embodiment). See Hilton-Davis, 62 F.3d at 1519.

Samsung has not argued that one of ordinary skill would lack knowledge of the interchangeability between [[C]] and a dedicated erase gate. In fact, the record establishes that other companies have used [[C]] instead of an erase gate as the terminal to which erase voltage conditions are applied to draw electrons off the floating gate during the erase operation. See FF III 44; CPFF 265-271; SPFF 102.

Indeed, [[C]] performs the same function (acting as a terminal for receiving erase voltage) in substantially the same way (creating a potential difference between [[C]] and the control gate) which pulls electrons off the floating gate to obtain the same result (removal of electrons from the floating gate) as the erase electrode referenced in claim 27. FF V 126-131.

Accordingly, if the erase electrode element is not literally satisfied by the [[C]] it is met under the doctrine of equivalents.

2. Increment/Decrement Element

[

[C]

] FF V 134-135. This feature alone satisfies the requirement of claim 27 that "a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions." See, *supra*, at 53-57. [

[C]

] FF V

136.

Samsung argues that its devices do not satisfy the increment/decrement element of claim 27 because [

[C]

] See Choi, Tr. 1351-1352. Moreover, Samsung's asserted claim construction, requiring that both erase and programming operations be effected by successive applications of voltage, was rejected above.

Accordingly, it is found that Samsung's devices practice this element of claim 27.

3. Temporary Storage Means

As discussed above, the element "means for temporarily storing a chunk of data for programming a plurality of addressed cells" requires data to be stored in a latch or equivalent structure at least until the cell is verified and programming to the cell is inhibited. [

[C]

] FF V 141-144.

Accordingly, Samsung's devices fall within the properly interpreted scope of this element.

Samsung's argument that its devices lack this claim element is based on an incorrect interpretation of the relevant claim language. In particular, Samsung contends that this element must be construed to require data to be stored "during the entire programming process." Respondents' Post-Hearing Br. at 22. That proposed construction of the claim was rejected above.

Samsung also argues that its devices [

[C]

] Respondents' Post-Hearing Br. at 23.

However, this argument is contradicted by Samsung's own technical documentation. [

[C]

] Id.

Although the terminology is somewhat different, the function carried out in Samsung's devices is the exact same function performed by the temporarily stored data in the '338 patent. See FF V 144; CX 2 ('338 Patent) at col. 19, line 42 through col. 20, line 16. Accordingly, Samsung's devices satisfy this means-plus-function element."

4. Parallel Programming Means

Both SanDisk's infringement expert and Samsung's infringement expert agree that Samsung's flash memory devices perform the function of programming

" [

[C]

] Respondents' Post-Hearing Br. at 23. As set forth above, these alleged differences do not place the Samsung devices outside the scope of this claim element. Aside from these "differences," [

[C]

satisfy the second prong of a "means-plus-function" analysis. FF V 142-144.], and

in parallel into the addressed cells." FF V 145-146.

Nevertheless, Samsung contends that its devices do not satisfy this element because they do not perform the programming function in the same manner as the Hot Electron Injection programming method described in the preferred embodiment of the '338 patent. However, as explained above, claim 27 contains no limitation as to the manner or method of programming. Indeed, from the perspective of the patented invention, there is no difference between programming using Fowler-Nordheim tunneling and programming using Hot Electron Injection inasmuch as both force electrons through the oxide onto the floating gate, which is all that is needed to program a flash memory.

Accordingly, it is found that Samsung's devices practice this claim element.

5. Verifying Means

Samsung's flash memory devices perform the function of "verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data." See FF V 152. [

[C]

" Samsung's devices do not have a source mux or drain mux as shown in Figure 14 of the '338 patent. FF V 148. However, because Samsung uses a NAND architecture, the functions of the muxes can be performed without using these structures. It is logical not to use such muxes in the Samsung designs. FF V 149-151. The logical elimination of these unnecessary structures does not affect the infringement analysis with respect to this means-plus-function claim element. See Data Line Corp. v. Micro Technologies, Inc., 813 F.2d 1196, 1202 (Fed. Cir. 1987) ("We conclude that a reasonable jury could have found that a single sensor with multiplex switching is the equivalent of multiple sensors with multiple switches, and that these are within the scope of the limitation 'means for sensing' in claim 1.").

] FF V 154.

The arguments by Samsung and OUII that Samsung's devices lack the claimed verifying means are based on a flawed interpretation of the relevant claim language. It is argued that the Samsung devices do not perform the function of "verifying the programmed data ... with the chunk of stored data" because [(C]

] See SPFF 305; RPFF 458. However, the '338 patent does not require verification of cells that are targeted to be in the erased state. Indeed, as detailed above, the '338 patent expressly states in the context of discussing the verification function that "if each memory cell is to store K states, then at least K - 1, or preferably K reference levels need be provided." CX 2 at col. 11, lines 56-58. In other words, in the case of a two state device, only a single reference level need be used for performing the verification function (i.e., where "0" equals the programmed state, the device only needs to determine whether the cell has reached the "0" state, and can ignore cells targeted to remain in the erased state). The '344 patent (which is incorporated by reference into the '338 patent) similarly discloses that a single sense amplifier and a single reference level can be used to differentiate between conduction states "1" (or erased) and "0" (or programmed).

As discussed above, before a flash EEPROM sector can be programmed, it must be erased. See FF V 158. As a result, all of the cells in the sector are necessarily in the erased state at the beginning of the programming process. In a binary implementation of the '338 patent, cells targeted to be in the erased state are then automatically inhibited from programming before

the first pulse is applied. FF III 68.⁹⁰ Thus, it would be obvious to anyone of ordinary skill in the art that there is no reason to verify repeatedly whether cells targeted to be in the erased state are in fact in the erased state, since absent a device failure, there is no way for such cells to come out of the erased state that they were in at the beginning of the programming cycle.⁹¹ FF III 71; Pathak, Tr. 823-831; Mehrotra, Tr. 342-351.

Accordingly, the evidence shows that Samsung's devices perform the "verify" function recited in the '338 patent.⁹²

Both Samsung and OUII argue that Samsung's devices do not satisfy the "means for verifying" element either literally or under the doctrine of

⁹⁰ Samsung has proposed a finding that: "Cells in the '338 patent that are to remain in the erase state never encounter programming conditions, and, therefore, there is no need to make a change in their programming conditions." See RPFF 479 (citing Harari, Tr. at 266).

⁹¹ Indeed, at the hearing, Samsung's expert Dr. Allen testified that the M293, a device alleged to invalidate the '338 patent, "does meet the language of the claim in '338," even though that device performed a verify operation "just in the case of going from zero to one." (i.e., only for cells targeted to be in the programmed state). Allen, Tr. 1179-1180; see also Gross, Tr. 1447-1452; CX 204 (concerning the fact that M293 only verifies cells targeted to be in the programmed state, and performs no verification on cells targeted to remain in the erased state). The same type of verification is performed by the Samsung devices. FF V 152-157.

⁹² Samsung also argues that it does not verify the programmed data with the chunk of stored data because it does not store "program data," and there is "no temporary storage of data for programming." Respondents' Post-Hearing Br. at 25. As set forth previously in connection with the temporary storage means, the differences between the Samsung devices and the '338 patent with respect to the storage of "program data" are largely semantic, while in other instances Samsung has in fact referred to the stored information as "program data." See CX 56. [

[C]

] See FF V 135, 153-154. This is precisely what is claimed in the '338 patent.

equivalents, because their circuitry is not equivalent to that described in the '338 patent.

As noted above, the '338 patent specifically contemplates a binary device in which a single reference level is used. See SPFF 133-134; CPFF 775. A person of ordinary skill seeking to implement Figure 11-E in a binary device with a single reference level (as is disclosed in the '344 patent at col. 11, lines 56-58) would only use a single sense amplifier to perform that function. See FF III 71-72. Moreover, in its discussion of Figure 11-E, the '344 patent specifically acknowledges that for a four-state device, "only three sense amplifiers and three reference levels are required to sense the correct one of four states," and that a single sense amp and a single reference level can be used to "differentiate correctly between conduction states '1' and '0'." FF V 163; CX 3 ('344 Patent) at col. 26, lines 51-60. Thus, the '344 patent explicitly teaches that for a binary device, only one sense amplifier and one reference level is required to sense the correct state. Finally, the '344 patent specifically discusses an embodiment of Figure 11-E in which "a single sense amplifier" is used. FF V 164; CX 3 at col. 26, lines 8-15. These disclosures are more than adequate to support the conclusion that Figure 11-E would be reduced to a single sense amplifier in a binary device, and that such a structure is the structural equivalent of Figure 11-E."

[

[C]

" The testimony of Samsung's expert, Dr. Allen, also supports this interpretation. Dr. Allen testified that one of ordinary skill in the art would use a single sense amplifier to verify the programming of a binary device. Dr. Allen further testified that the M293, which uses a single sense amplifier (and no comparator circuit) to perform the verify operation, satisfies the "means for verifying" element of claim 27. Allen, Tr. 1173-1180; see also FF III 71, IV 136.

[C]

] FF V 154. As set forth above, this structure is identical to, or at the very least the structural equivalent of, the structures disclosed in the '338 patent for binary simplifications of Figure 11-E. FF V 155-157. Accordingly, Samsung's devices satisfy this element as properly construed.

6. Inhibiting Means

Samsung uses [[C]] to perform the function of "inhibiting further programming of correctly verified cells among the plurality of addressed cells." The latch used by Samsung is equivalent to latch 721 in Figure 16 of the '338 patent. See FF V 166-171.

Samsung argues that it does not practice this element because it performs the claimed function in a different manner than the preferred embodiment in the patent. This claim element is written in means-plus-function form. The law provides that if an accused device employs a structure that is identical or equivalent to that disclosed in the specification in order to perform the identical function required in the claim, then infringement will be found. Valmont, 983 F.2d at 1042." Claim 27 contains no limitation concerning the manner in which a covered structure is to operate, and Samsung has provided no legal basis upon which to find that infringement may be avoided because of the manner in which the structure operates.

Indeed, Samsung's devices perform the function of inhibiting further

" See also Intel Corp., 946 F.2d at 842; D.M.I., Inc. v. Deere & Co., 755 F.2d 1570, 1575 (Fed. Cir. 1985).

programming of a correctly verified cell, until all cells in the chunk have been verified. Pathak, Tr. 840-846; SPFF 312. As in the '338 patent, the inhibiting function is accomplished in Samsung's products [

[C]

] SPFF 313.

[

[C]

] Thomas, Tr. 1119-1120; SPFF 315. In contrast, flipping the latch 721 disclosed in the '338 patent causes 0 volts to be applied to the drain of the disclosed NOR cell. FF V 177; SPFF 316. Nevertheless, no additional structure is required with respect to the latch 721 in order to accomplish the inhibiting function claimed in the '338 patent. Samsung's products therefore include the inhibiting means recited in claim 27.

7. Final Means-Plus-Function Element

In denying that it practices the final element of claim 27, Samsung's only argument is that this final element incorporates three previous elements (parallel programming means, means for verifying, and means for inhibiting further programming) that Samsung contends are not present in its devices. Respondents' Post-Hearing Br. at 27-28. Inasmuch as Samsung practices those three claim elements, Samsung also practices this final claim element. See FF V 179-183.

Conclusion

Based on the foregoing analysis of Samsung's devices, the Administrative Law Judge finds that Samsung infringes claim 27 of the '338 patent literally, or in the alternative, under the doctrine of equivalents.

B. Construction of Claim 27 of the '338 Patent

39. Claim 27 of the '338 patent is as follows:

In an array of addressable semiconductor electrically erasable and programmable memory (EEPROM) cells on an integrated circuit chip, the memory cell being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltage conditions for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions, a system for programming data to EEPROM cells including means for temporarily storing a chunk of data for programming a plurality of addressed cells, means for programming in parallel the stored chunk of data into the plurality of addressed cells, and means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data, wherein the improvement comprises:

means for inhibiting further programming of correctly verified cells among the plurality of addressed cells; and means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly.

CX 2/RX 5 ('338 Patent) at col. 26, lines. 28-54.

40. The term "erase electrode" is found in the '338 patent only in the claims. CX 2; see CFF 257; SFF 98.
41. The term "electrode" is commonly understood in the semiconductor industry as a terminal to which an electrical signal is applied to perform some function. Pathak, Tr. 792, 918.
42. An "erase electrode" is understood in the semiconductor industry as a terminal to which erase voltage conditions are applied to draw electrons off the floating gate. Pathak, Tr. 792.
43. Various structures or terminals in a flash memory device can function

- also as an erase electrode as that term would be commonly understood, including the silicon substrate. Harari, Tr. 77-83.
44. Various companies have used the substrate instead of an erase gate as the terminal to which erase voltage conditions are applied to draw electrons off the floating gate during the erase operation. Harari, Tr. 77-83; CPX 25.
45. The word "or" in this instance serves its normal function of indicating the availability of an alternative or a choice. See Webster's at 1585.
46. The increment/decrement element of the preamble of claim 27 corresponds to the programming algorithm illustrated in Fig. 15 (item 6), which is described in the text at col. 19, line 57 through col. 20, line 16), whereas the erasing algorithm is illustrated separately in Fig. 11 (items 1 and 2), which is described at col. 16, lines 18-25.
47. The preferred embodiment disclosed in the specification provides examples of incremental programming and of incremental or decremental erasing. See CX 2 at col. 18, lines 21-29.
48. The application of voltage conditions for programming and the application of voltage conditions for erasing are independent of each other. Harari, Tr. 1861, 1870.
49. In both binary and multistate devices, one may design for incremental programming and/or for incremental erasing. However, programming and erasing are not part of the same operation. Harari, Tr. 1869; Pathak, Tr. 937.
50. The consequences of over-erasing are endurance-related. The effect of over-erasing, even in a multistate device, is not catastrophic to the performance of the device. Harari, Tr. 1870; Guterman, Tr. 577-578.

51. With respect to the '338 patent, after the programming of a cell is completed, the information used to program that cell is not used again. Harari, Tr. 248-249.
52. The term "temporarily" ordinarily means "for a brief period: during a limited time: briefly." Webster's at 2353.
53. The "temporarily storing" means of claim 27 is disclosed in Figure 5, including block 190 (labeled "Read/Program Latches and Shift Registers"). Harari, Tr. 247-249; Thomas, Tr. 1509-1511; CX 2, at col. 19, line 27 through col. 20, line 36.
54. The data may be stored in the latches until verification has occurred for the entire chunk of data stored therein, although there is no express requirement to that effect. Thomas, Tr. 1510-1511; Pathak, Tr. 939.
55. After a particular cell to be programmed is verified, the data stored in the latch 190 serves no function for the cell that is already programmed, while the programming continues for the rest of the chunk. Harari, Tr. 247-249; Mehrotra, Tr. 329; Guterman, Tr. 587-588.
56. One of ordinary skill in the art knows that once programming and verification has taken place, the job is done, and "temporarily" in that case would mean just until the job is done. Pathak, Tr. 940-944.
57. Figure 14 of the '338 patent discloses certain structures with which the parallel programming function required by the preamble of claim 27 can be performed. CX 2 at col. 5, lines 40-41; col. 19, lines 27-41; Mehrotra, Tr. 330.
58. In particular, Figure 14 shows an embodiment in which a Program Circuit with Inhibit, block 210, performs the parallel programming function, with the source multiplexer (or "mux") 107 and the drain mux

109 providing the data path. CX 2 at col. 19, lines 27-41; Mehrotra, Tr. 330-334.

59. The cells in the preferred embodiment of the '338 patent are connected in a NOR architecture configuration. Pathak, Tr. 812-813.
60. HEI programming is thus appropriate for use with the cells described in the preferred embodiment. Harari (Tutorial), Tr. 51-52; Mehrotra, Tr. 334-335.
61. The language of claim 27 is silent on the cell structure and the corresponding programming method that must be used. It merely recites the broad, general function of "programming in parallel" without specifying how that programming occurs. One of ordinary skill in the art would know that parallel programming can be achieved through more than one method depending on the type of cell structure selected in a device. Furthermore, circuit designers are familiar with the various methods of programming cells depending upon their structures. Pathak, Tr. 944-946; Harari, Tr. 1861-1865.
62. In claim 27 of the '338 patent, "programming in parallel" means that programming takes place for more than one cell at a time, such that all cells selected for programming by a chunk of data receive programming conditions at the same time. See Harari, Tr. 76; Pathak, Tr. 807-808; CX 2 at col 19, lines 30-31 ("The EProm array 60 is addressed by N cells at a time.").
63. The term "verifying" as it is used in claim 27 of the '338 patent normally would be understood by one of ordinary skill to refer to the process of determining whether the data in a memory cell matches the data that is targeted to be written into the cell. Guterman, Tr. 489-490, 499. There is no contrary definition of the term in the '338

patent. CX 2.

64. Mr. Thomas, Respondents' expert on whether Complainant SanDisk practices the '338 patent and on whether Samsung infringes the '338 patent, testified that the term "verify" is ordinarily used very loosely in the semiconductor industry to refer to the process of determining whether a cell is finished programming. Thomas, Tr. 1594-1595.
65. In a multi-state device, such as that described in the '338 patent's specification, a cell can be in one of several states. In performing the verification function, the first step is to determine the state of the cell to be verified (e.g., 0, 1, 2, 3). After determining the state the cell is in, the next step is to determine whether the cell is in the target state for that cell. If the cell is in the target state, the cell is verified; if not, further programming is required. Guterman, Tr. 490-493; CPX 46.
66. In a binary device, before programming can begin all cells must be in the erased state. Guterman, Tr. 493-495; CPX 48.
67. Inasmuch as all cells start in the erased state, if the targeted state of a particular cell is the erased state, then the cell is in the targeted state before the programming cycle begins, and therefore no further action needs to be taken with respect to that cell. Harari, Tr. 264-265; Guterman, Tr. 493-495, 499-503; CPX 48.
68. If the targeted state of a particular cell is the programmed state, and if the cell is not in the targeted state before the programming cycle begins, then programming pulses must be applied to bring the cell to its targeted state. Guterman, Tr. 493-495; CPX 48. For cells targeted to be in the programmed state, the cell is read after each programming pulse to verify whether the cell is in the programmed state

(i.e., reads a "1"). Once the cell is sensed to be in the programmed state, further programming to that cell is terminated. Guterman, Tr. 493-495; CPX 48.

69. Figure 11-E of the '344 patent (which is incorporated by reference into the '338 patent) discloses circuitry that corresponds to the verify means in a multi-state implementation of the claim 27 invention. Figure 11-E depicts a multi-state implementation for a single cell in which the cell is able to hold one of four states. CX 2 at col. 4, lines 23-30; Guterman, Tr. 498-499; CX 3 (the '344 Patent); CPX 64.
70. Figure 11-E of the '344 patent discloses four sense amplifiers, one associated with each of the four states that the cell can hold. Each of the four sense amplifiers senses whether the current passing through the cell is greater or lesser than the reference current corresponding to the state associated with that sense amplifier. In the multi-state embodiment disclosed in Figure 11-E, once the sense amplifiers perform their sensing operation, the results are fed into the comparator disclosed in Figure 11-E, which determines whether the state of the cell matches the targeted state of the cell. Guterman, Tr. 499-503; CX 3, Fig. 11-E.
71. A binary embodiment equivalent to that disclosed in Figure 11-E of the '344 patent would not need all the circuitry disclosed in that Figure for a multi-state implementation. Guterman, Tr. 499-503. In a binary device, it is unnecessary to have more than one sense amplifier to perform the verification function of claim 27, since the only decision or verification that the device has to make is whether the cell is in the programmed state. Guterman, Tr. 499-503; Allen, Tr. 1173; CPX 64, 66.

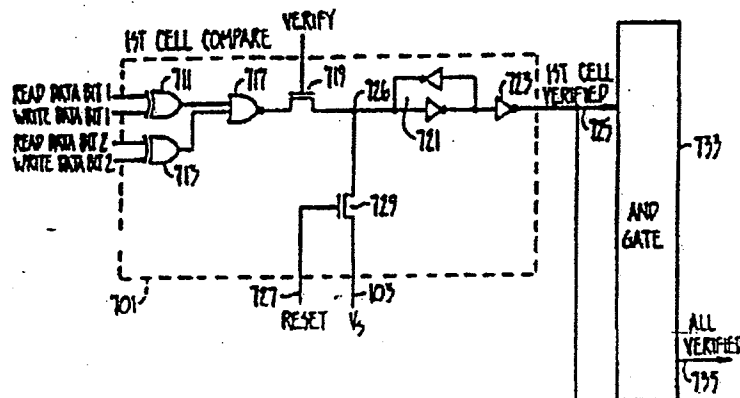
72. For a binary device, it would be logical for a circuit designer to simplify the structure of Figure 11-E of the '344 patent by eliminating three of the four sense amplifiers and the buffers and circuitry uniquely associated with those sense amplifiers, since they serve no function in a binary device and unnecessarily occupy surface area on the chip. Furthermore, with a single sense amplifier, it is unnecessary to have a separate comparator circuit, since that comparator would merely replicate the function of the sense amplifier. Guterman, Tr. 499-503; CPX 64; CPX 66.
73. Figure 16 of the '338 Patent discloses certain additional structures for performing the verification function in a multi-state device. In the circuit compare module 703 shown in the Figure, the read bits are compared bit by bit with corresponding program data bits, i.e., it is determined whether there is a match between the read and write data. This is performed by XOR (exclusive OR) gates such as 711, 713 and 715 shown in Fig. 16. The specification states that the number of such XOR gates used depends upon the number of binary bits encoded for each cell. The output of the XOR gates passes through a NOR gate 717 whenever all the bits are verified, and node 726 is taken high so that latch 721 is set in the verified state. Once latch 721 is set, the cell inhibited from further programming during subsequent programming pulses that may be applied on the chunk. If, however, the read data does not match the write data, then latch 721 remains in its previous state. Mehrotra, Tr. 339; CX 2 at col. 20, lines 17-51.
74. The '344 patent expressly discloses that a single sense amplifier and a single reference level can be used to differentiate between conduction states "1" (which could indicate "programmed") and "0" (for "erased").

CX 3 at col. 26, lines 55-60. The '344 patent teaches that in a four-state storage device the comparison may be accomplished with four consecutive read cycles and only one sense amplifier, with a different reference applied at each cycle, if the additional time required for reading is not a concern. CX 3 at col. 25, line 64 through col. 26, line 17.

75. The Figure 16 multi-state embodiment could be modified for a binary device by making some simplifications to the structures that would be obvious to an ordinary flash memory circuit designer. Mehrotra, Tr. 342; Pathak, Tr. 819-820.
76. The '338 patent contemplates an embodiment with only two states. The '338 Patent expressly states in the context of discussing the verification function that "if each memory cell is to store K states, then at least $K - 1$, or preferably K reference levels need be provided. In one embodiment, the addressed cell is compared to the K reference cells using k sense amplifiers in parallel. This is preferable for the 2-state case because of speed" CX 2 at col. 11, lines 56-61.
77. It would be obvious to a circuit designer of ordinary skill to eliminate all but one of the XOR gates (711, 713, 715) in a binary device, since only one bit is being stored in the cell (i.e., "L" = 1). Mehrotra, 342-343; CPX 120; Pathak, Tr. 820-822; CPX 122.
78. In a binary device, it would be obvious to a circuit designer of ordinary skill to change NOR gate 717 of the '338 patent to a single inverter, since there would only be a single XOR gate, and therefore only a single input. Mehrotra, Tr. 342-345; CPX 120; Pathak, Tr. 820-822; CPX 122.
79. In implementing Figure 16 of the '338 patent in a binary device, the

possible combinations of read (R) and write (W) are greatly reduced, as compared to a multi-state device, such that it is not necessary to implement the logic inherent XOR (exclusive OR) gates and NOR gates to verify a cell. Thus, one would expect to make additional simplifications to the circuitry shown in Figure 16 by eliminating entirely the XOR gates and the NOR gate 717. Mehrotra, Tr. 345-351; CPX 120; Pathak, Tr. 819-829; CPX 122; CPX 127; CPX 128.

80. In a binary device, there are only four logically possible states: R=0 and W=0; R=0 and W=1; R=1 and W=0; R=1 and W=1. For example, in the first scenario (R=0 and W=0), the data read from the memory is zero (erased) and the data desired to be written into the memory is also zero. Note also that the third scenario (R=1 and W=0) should not be possible because all cells are required to be in an erased state before programming starts. Mehrotra, Tr. 345-346.
81. Figure 16 of the '338 patent discloses one embodiment of the compare circuit used in the multi-state, preferred embodiment. Figure 16 also discloses circuitry that inhibits further programming of the memory cells. CX 2 at col. 20, line 17-18; Mehrotra, Tr. 340.
82. The pertinent circuitry is depicted in Figure 16 of the '338 as follows:



This illustration, like the illustration contained in Respondents' reply brief, depicts the circuitry of one compare module contained in the preferred embodiment (compare module 701). Figure 16 and the text of the specification provide for "N compare modules such as 701, 703, one for each of the N cells in the chunk." CX 2 at col. 20, lines 18-20, Fig. 16.

83. In the circuit shown in Figure 16, a latch 721 performs the function of inhibiting further programming to correctly verified cells.

Mehrotra, Tr. 340-342.

84. When a cell is correctly verified, the result is sent to latch 721, which is then set to the verified state. Mehrotra, Tr. 340; CX 2 at col. 20, lines 28-32.

85. The specification mentions that at the end of a programming pulse all the latches are reset to the unverified state. Node 726 can only be reset by transistor 729 and not by node 717 after node 726 goes high. Mehrotra, Tr. 371-372. Once latch 721 is set in the verified state, the cell is inhibited from further programming during any subsequent

- programming pulses which may be applied. Latch 721 in Figure 16 is a "one-way latch." Mehrotra, Tr. 340.
86. The '338 patent specification teaches that "[p]rogramming and verification are repeated until all the cells are correctly verified." FIG. 15(7). Thus, each cell must be read to determine whether the read and write data for that cell match. The specification does not teach that the verification process is to occur repeatedly, *i.e.*, after a cell has been verified. CX 2 at col. 20, lines 14-16.
87. Latches are often referred to as "one-way" or "two way." One-way latches and two-way latches are often drawn in the same manner. Mehrotra, Tr. 372, 397. Yet, they function differently. A two-way latch freely switches back and forth between two states when different input values are applied. Thus, if the input to the latch is a 0, then the value saved in the latch becomes a 0. If a subsequent input is a 1, the latch then saves a 1. However, a one-way latch is said to move in only one direction. Allen, Tr. 1077.
88. With a one-way latch, when verification occurs and the latch is set to a "1", the latch does not go back to a zero during the overall cycle of iterations. Allen Tr. 1078.
89. A one-way latch like that used in Figure 16 of the '338 patent will not allow the detection of so-called "program disturb conditions" where, due to defects in a part, a cell goes back to an erased state before the entire chunk of data is verified. Nor will a one-way latch allow the detection of conditions in which a part fails and a cell is disturbed from an erased into a programmed state. Harari, Tr. 250-252; Mehrotra Tr. 374-378; CX 2.
90. Neither claim 27 of the '338 patent, nor the specification mentions

the detection of program disturb conditions. CX 2.

91. With respect to Figure 16, the specification teaches that the output of the XOR gates passes through NOR gate 717 such that a "1" appears at the output of NOR gate 717 whenever all the bits are verified, otherwise a "0" appears there. When verification occurs (i.e. "[w]hen the control signal VERIFY is true"), "this result is latched to latch 721 such that the same result at the output of NOR gate 717 is also available at the cell compare module's output 725." CX 2 at col. 20, lines 25-32 (emphasis added). The output 725 is fed through an output line to the "program circuit with inhibit 210 of FIG. 5." CX 2 at col. 20, lines 33-36.
92. The specification in describing the functions of latch 721 states that "[w]hen the control signal VERIFY is true, this result is latched to latch 721." It says nothing about resetting latch 721 in case of a subsequent (or previous) control signal VERIFY that is not true. Thus, the specification does not provide that it will return to an unverified state during the program and verification of a chunk of data. Indeed, since latch 721 is a one-way latch, once the latch is set, the stored data cannot be affected by the output of NOR gate 717. Mehrotra, Tr. 340-341.
93. The preferred embodiment of the '338 patent is a multi-state device. If latch 721 were not a one-way latch, there would be catastrophic failure of the multi-state device. See McGreivy, Tr. 1697-1708, 1793-1813; CX 2 at col. 19, lines 4-26.
94. The specification provides that in order to change the setting of latch 721:

At power-up or at the end of program/verify of a chunk

of data, all cell compare module's outputs such as 725, 727 are reset to the "not verified" state of "0". This is achieved by pulling the node 726 to V_{ss} (0 V) by means of the RESET signal in line 727 to a transistor 729.

CX 2 at col. 20, lines 46-51.

95. If latch 721 were a two-way latch, before the commencement of programming a cell would be read and if found not to be in the correct state, latch 721 would flip back to the not verified state in response to the output of NOR gate 717, and it would not be necessary to reset the latch with the reset signal. Mehrotra, Tr. 399-400.
96. The specification shows that latch 721 can only be reset by the effect of transistor 729. See Mehrotra, Tr. 342. The specification demonstrates that latch 721, once set to the verified state, remains in the verified state during the entire program/verify of a chunk of data. Then, latch 721 is returned to the "not-verified" state by a reset operation in which node 726 is pulled down, as one would expect in the case of a one-way latch. See Mehrotra, Tr. 400; See also, Allen, 1079, 1086.
97. In order to pull down latch 721, one would have to design the circuit shown in Figure 16 to have transistors of the proper size. Mehrotra, Tr. 409; see also Allen Tr. 1079. The '338 patent does not indicate the size of the transistors involved in Figure 16. Nonetheless, one of ordinary skill would know how to size the transistors shown in Figure 16 relative to the size of NOR gate 717 so as to achieve a one-way latch. CX 2; Mehrotra Tr. 404-409.
98. In addition to the disclosure of Figure 16, including latch 721, Figure 5 of the '338 patent contains a block 210 entitled "Program Circuit with Inhibit." This block provides no detail regarding the

specific circuitry that actually inhibits further programming. CX 2; Guterman, Tr. 508-510.

99. Figure 17 shows "one embodiment of the program circuit with inhibit 210 of Fig. 5 in more detail." CX 2 at col. lines 52-53. The one embodiment shown in Figure 17 is relevant to the Hot Electron Injection programming method used in the preferred embodiment. The circuitry in Figure 17 is for removing voltage from the drain of a cell to inhibit further programming. CX 2, col. 20, line 52 through col. 21, line 8; Mehrotra, Tr. 352-353; Guterman, Tr. 511-513.
100. To one skilled in the art, one way of implementing the inhibit means is to combine certain disclosures in Figures 16 and 5, in particular block 190 of Figure 5, which is entitled "Read/Program Latches and Shift Register." The temporary storage latch disclosed in block 190 of Figure 5 can also serve as the inhibit latch 721 of Figure 16 of the '338 Patent. Mehrotra, Tr. 349-351; CPX 120; CX 2, Fig. 16; Pathak, Tr. 835-839; CPX 57C-58C; CPX 124-125.
101. A flash memory designer of ordinary skill would seek to combine the functions of the temporary storage latch and the verify inhibit latch in a single structure in order to save transistors, thereby reducing the surface area of the chip. Pathak, Tr. 839-840.
102. Figure 16 of the '338 patent discloses structures that correspond to the final means-plus-function element of claim 27 in a multi-state implementation. Those structures include the one-way latch 721, the outputs such as output 725, as well as AND gate 733 whose single output 735 is used to signal the controller in the preferred embodiment that all cells in the chunk of data have been correctly verified. Mehrotra, Tr. 341; CX 2 at col. 20, lines 18-51.

103. The specification provides in part: "[a]s soon as the programmed state is verified correctly, programming stops." CX 2 at col 18, lines 24-25.
104. The patent provides that "parallel programming is implemented in the preferred embodiment of the '338 Patent by a selective programming circuit which disables programming of those cells in the chunk that have already been verified correctly." CX 2 at col. 19, lines 13-16.
105. The patent also provides that "it is preferable to apply programming voltages in repetitive short pulse with a read operation occurring after each pulse to determine when it has been programmed to the desired threshold voltage level, at which time the programming terminates." CX 2 at col. 9, lines 13-18.
106. Each of the specification passages cited above clearly indicate that the '338 patent will not apply an additional programming pulse to a cell after it has been verified. See Mehrotra, Tr. 253-254; McGreivy, Tr. 1693-1696.
107. Dr. McGreivy explained that failure to terminate will, over time, overstress a binary device and make a multi-state device malfunction. McGreivy, Tr. 1697-1708, 1793-1813. This point is addressed in the text of the '338 patent, as follows:

In the prior art EEPROM devices, after each programming step, the state attained in the cell under programming is read and sent back to the controller 140 or the CPU 160 for verification with the desired state. This scheme places a heavy penalty on speed especially in view of the serial link.

In the present invention, the program verification is optimized by programming a chunk (typically several bytes) of cells in parallel followed by verifying in parallel on chip. The parallel programming is implemented by a selective programming circuit which disables programming of those cells in the chunk whose states have already been verified correctly. This

feature is essential in a multi-state implementation, because some cells will reach their desired state earlier than others, and will continue pass [sic] [past] the desired state if not stopped. After the whole chunk of cells have been verified correctly, logic on chip communicates this fact to the controller, whereby programming of the next chunk of cells may commence. In this way, in between each programming step data does not need to be shuttled between the EEprom chip and the controller, and program verification speed is greatly enhanced.

CX 2 at col. 19, lines 4-26.

know, depending on the type of technology and cell he was working with, whether to apply a resistor, charge pump or some other circuit to apply the erase voltage to the selected sectors. Mehrotra, Tr. 387-388; McGreivy, Tr. 1651-1652.

93. According to Dr. Allen, a person of ordinary skill in the art that pertains to the Mitsubishi `997 patent has the same level of skill as that which pertains to the `752 patent, and provides enough information to enable a person of ordinary skill in the art to construct a EEPROM system as disclosed in the `752 patent; yet, the Mitsubishi Patent does not disclose any circuit mechanism for generating an erase voltage. Allen, Tr. 1135-1136.

94. [RESERVED]

95. [RESERVED]

96. Samsung's expert, Dr. Allen, admitted that the `752 patent is a logic level disclosure. Allen, Tr. 1003-1004, 1122.

97. Dr. Allen admitted that one of ordinary skill in the art of the `752 patent would know to use AND circuitry to connect the two signals coming into the sector selected for erase. Allen, Tr. 1123-1125, 1128-1129.

B. The `338 Patent

Anticipation

The M293

98. Samsung introduced an M293B1 television tuner device manufactured by SGS Thomson ("the M293") as a potentially relevant item of prior art. RX 309.
99. The M293 does not perform the function of permanently "inhibiting the programming of correctly verified cells until all the plurality of addressed cells are verified correctly" as required by the last element

- of claim 27. McGreivy, Tr. 1691-1693, 1793-1794; RT 1818, 1830-1831, 1843; RX 180 at 12-13 and Exh. 1, Sheet 7; CPX 73; CX 199; RX 71.
100. The M293 permits the application of additional programming pulses to an already verified cell. McGreivy, Tr. 1691-1693, 1793-1794; Mehrotra, Tr. 1818, 1830-1831, 1843; Gross, Tr. 1453-1454; RX 180. at 12-13 and Exh. 1, Sheet 7; CPX 73; CX 199; RX 71.
101. The M293 "conditionally" or "temporarily" inhibits the programming of verified cells on a pulse-by-pulse basis. Gross, Tr. 1453-1454; RX 180 at 12-13 and Exh. 1, Sheet 7; McGreivy, Tr. 1691-1693, 1793-1794; Mehrotra, Tr. 1818, 1830-1831, 1843; CPX 73; CX 199; RX 71; CPX 73; CX 199.
102. The M293 does not possess any structure that is capable of permanently inhibiting the programming of correctly verified cells. Allen, Tr. 1115; RPX 43; RX 180, at 12-13, Exh. 1, Sheet 7; McGreivy, Tr. 1687-1690, 1691, 1787-1788; CX 199.
103. The M293 device does not possess the one-way latch that is disclosed in circuit 721 of Figure 16 of the '338 patent. Allen, Tr. 1115; RPX 43, RX 180, at 12-13, Exh. 1, Sheet 7; CX 2, at Fig. 16.
104. The "temporary" or "conditional" inhibit present in the M293 would not function for a multistate device. McGreivy, Tr. 1699-1701.
105. The permanent inhibition of verified cells disclosed in the '338 patent is critical to the successful operation of multistate devices. McGreivy, Tr. 1699-1701, 1706.
106. The element in claim 27 which requires permanently inhibiting the programming of verified cells is beneficial to binary NAND devices. Harari, Tr. 73, 1863-1865, 1867-1868; Choi, Tr. 1409.
107. CX 204 is a true and correct copy of a report entitled "An Analysis of

- SGS Thomson M293B1 EPM32: Electronic Program Memory for 32 Stations" that was prepared by Chipworks, Inc. ("Chipworks Report"). CX 204.
108. The Chipworks Report is an analysis of the SGS Thomson M293 device that was jointly commissioned by SanDisk and Samsung. CX 204, cover page.
109. The Chipworks Report was the result of extensive reverse engineering analysis of relevant internal circuits of the M293. CX 204 at 1.
110. The Chipworks reverse engineering analysis included a review of the following documentation: (1) the TAEUS Technology Analysis Report entitled "SGS M293 Electronic Program Memory Device ("TAEUS Report") (RX 180C); (2) M293 Data Sheet (RX 98); (3) SGS Technical Note 153 (RX 96); and (4) an article by Guido Torelli entitled "An Improved Method For Programming A Word-Erasable EEPROM" ("Torelli Article"). CX 204 at Tabs 5-8.
111. The Chipworks reverse engineering analysis included removal of the plastic package surrounding the chip and photographing of the relevant circuits. CX 204 at 12, Tab 2.
112. The Chipworks analysis included the microprobing of the internal bit lines of the M293 in order to observe the voltage waveforms during programming and read cycles. CX 204 at 12.
113. In order to microprobe, it was necessary for Chipworks to (1) jet etch a hole through the plastic package to expose the die and (2) remove the scratch protection layer by a wet acid etch to allow direct contact to the metal interconnect lines. CX 204 at 12.
114. The test jig used by Chipworks to test the M293 was constructed around a 28-pin ZIF socket to hold the M293 during the test. CX 204 at 12.
115. In the morning test session of October 15, 1996, the probe tip used to

contact a bit line was connected to a Tektronix TDS380 digital real time oscilloscope via a 10x attenuating probe having an impedance of 14.1 pF and 10 Megaohms. CX 204.

116. In the afternoon test session of October 15, 1996, the oscilloscope was changed to a Tek TDS700A series unit with a 10x attenuating probe of higher impedance: 8.0pF and 10 Megaohms. CX 204.

117. A single M293 device was used for all measurements. CX 204 at 13.

118. Only one bit line was probed for any given measurement depicted in the waveforms attached to Tab 4 of the Chipworks Report. CX 204 at 13, Tab 4.

119. Electrical tests and measurements were made on 6 arbitrary bit lines. CX 204 at 13.

120. All electrical measurements were made at room temperature. CX 204 at 13.

121. The electrical test measurements were made in a semi-darkened room to reduce the light striking the die to a very low level. CX 204 at 13.

122. The test procedures used by Chipworks were agreed to by both SanDisk and Samsung.

123. Both SanDisk and Samsung had representatives present when Chipworks performed the electrical testing.

124. The Chipworks Report confirms the testimony of Dr. Allen and Dr. McGreivy that the M293 does not possess a structure to permanently inhibit programming. Allen, Tr. 1115; McGreivy, Tr. 1687-1690, 1691, 1787-1788.

125. In the M293, the programming of the selected cell on each column of the array is done by applying a sequence of high voltage programming pulses ("Vpp"). CX 204 at 4.

126. During programming, each individual programming pulse to a cell in the M293 device is followed by a verify read operation. CX 204 at 4.
127. When the M293 is in programming mode, the result of the verify read is retained only until the time of the next potential programming pulse. CX 204 at 4.
128. The verify read of the M293 only controls the application or inhibit of a single programming pulse. CX 204 at 4.
129. Programming in the M293 device stops when only all the cells are verified. The M293 does not possess any structure for permanently inhibiting the programming of correctly verified cells. CX 204 at Fig. A.
130. The M293 does not possess a structure to generate a program "lock-out" signal that will guarantee that no further programming will occur once a verify read operation reads a "1" (i.e., the cell has achieved its target programming state) for the first time. CX 204 at 4.
131. The M293 does not possess any structure to guarantee that no further programming will occur to a cell after a verify read operation reads a "1" for the first time. CX 204 at 4.
132. In the M293, it is possible that after one programming pulse has been inhibited, a subsequent pulse will be allowed on the previously verified and inhibited cell. CX 204 at 4.
133. The M293 stops programming altogether when the verify read operation results in "all one" being read across all bits (cells) of the selected word. CX 204 at 4.
134. The results of the Chipworks Report (the M293 does not permanently inhibit) is fully consistent with the results of (1) the SanDisk test report of the M293 and M296 (CX 199) and (2) TAEUS Report (RX 180C).

Compare CX 204 with CX 199 and RX 180C.

135. The application of an additional programming pulse to an M293 cell that has already been verified is possible if the cell has been programmed into a voltage region which produces a sense amplifier misread. CX 204 at 5-6.
136. The M293 uses a sense amplifier to "read" the state of the cell to determine whether a cell being programmed has achieved the "1" or programmed state. CX 204 at 2, 5-6.
137. Any sense amplifier has a small region of input voltages where the resulting output is uncertain and a misread is possible. CX 204 at 5-6.
138. During programming operations, the M293 applies a programming pulse whenever the cell being programmed reads a "0". CX 204 at 9.
139. In the M293, for those cells that read as a "1" (or the "programmed" state), the programming inhibit circuit prevents programming transistor T1 from being turned on and applying a high voltage to the cell. CX 204 at 2-3, 7, 9.
140. The electrical tests of the M293 conclusively show that the M293 does not possess a lock out that guarantees that additional programming pulses will not be applied to a cell after it has been verified. CX 204 at Tab 4.
141. Each and every waveform generated for the Chipworks Report show that the M293 can apply an additional programming pulse to a cell that has been previously inhibited. CX 204 at Tab 4.
142. The capacitive loading of the testing equipment used by Chipworks could cause a misread of an "almost 1" cell as a "1" subsequent to the programming pulse. CX 204 at 9.
143. The misread of an "almost 1" cell is immaterial to the Chipworks

analysis because it does not affect the conclusion that the M293 does not possess any structure for permanently inhibiting the programming of verified cells. CX 204 at 4

144. For an "almost 1" cell that is incorrectly inhibited from programming, the inhibiting of the programming pulse eliminates the high voltage charge on the loaded bit line to bias the next verify read and allows the cell to be correctly read as a "zero." CX 204 at 9.
145. Using the Chipworks test set-up for the M293, if a cell is inhibited for two or more programming pulses, the application of an additional programming pulse cannot be attributed to the capacitive loading of the test set-up. CX 204 at 9.
146. Using the Chipworks test equipment and set-up for the M293, an electrical test where a cell is inhibited for two consecutive pulses and then has a high voltage applied to it during the application of the third programming pulse necessarily indicates that the cell had been programmed into a region where the sense amplifier read result is uncertain. CX 204 at 10.
147. Tab 4, Trace 10 of the Chipworks Report shows a programming cycle where the M293 inhibited the cell being measured for two consecutive programming pulses before applying an additional programming pulse. CX 204 at 10, Tab 4, Trace 10.
148. Tab 4, Trace 10 of the Chipworks Report shows an electrical waveform that was made under test conditions where the high voltage pulse V_{pp} was set to 23 volts. A V_{pp} of 23 volts is 1 volt under the data book specifications. CX 204 at 10, Tab 4, Trace 10; RX 98.
149. Tab 4, Trace 10 of the Chipworks Report shows that after inhibiting two consecutive pulses, the M293 applied an additional programming pulse

to the cell. CX 204 at 10, Tab 4, Trace 10.

150. Tab 4, Trace 12 of the Chipworks Report shows an electrical waveform that was made under test conditions where the high voltage pulse Vpp was set to 24 volts. CX 204 at 10, Tab 4, Trace 12.

151. A high voltage Vpp of 24 volts is within the parameters recommended by the M293 data book. RX 98.

152. Tab 4, Trace 12 of the Chipworks Report shows a programming cycle where the M293 inhibited the cell being measured for two consecutive programming pulses before applying an additional programming pulse. CX 204 at 10, Tab 4, Trace 12.

The Torelli Article

153. Samsung introduced an article authored by Guido Torelli, et. al., entitled "An Improved method for programming a word-erasable EEPROM" (the "Torelli Article"), as a potentially relevant article of prior art. RX 71.

154. The Torelli Article described the operation and characteristics of the M293 device. Allen, Tr. 1044-1046.

155. The Torelli Article does not disclose the function of permanently inhibiting the programming of correctly verified cells. Allen, Tr. 1175-1177; McGreivy, Tr. 1687-1690; RX 71 at 490 and Fig. 4; CPX 73.

156. The Torelli Article does not suggest to an individual of ordinary skill in the art the function of permanently inhibiting the programming of correctly verified cells. Allen, Tr. 1175-1177; McGreivy, Tr. 1687-1690; RX at 490 and Fig. 4; CPX 73.

157. The Torelli Article, specifically Figure 4, indicates that the cells being programmed are verified between each and every programming pulse. McGreivy, Tr. 1687-1690; CX 86, at Fig. 4; CPX 73.

158. At most, the Torelli Article, specifically Figure 4, discloses a device that conditionally inhibits the programming of cells on a pulse-by-pulse basis. McGreivy, Tr. 1687-1690; CX 86 at Fig. 4; CPX 73.
159. The Torelli Article does not disclose any structure that is capable of permanently inhibiting the programming of correctly verified cells. Allen, Tr. 1038, 1192; McGreivy, Tr. 1689; RX 71 at Fig. 2.
160. The Torelli Article does not disclose any structure, like a one-way latch, that is capable of remembering whether a cell has been previously verified and inhibited during the application of previous programming pulses. Allen, Tr. 1038, 1192; McGreivy, Tr. 1689; RX 71 at Fig. 2.
161. The Torelli Article does not disclose any structure for temporarily storing a chunk of data for programming a plurality of addressed cells. Allen, Tr. 1020, 1191; McGreivy, Tr. 1759; RX 71 at Fig. 2.
162. The Torelli Article does not indicate whether the temporarily stored data is to be stored on or off chip. McGreivy, Tr. 1759, 1762; RX 71 at Fig. 2.
163. The Torelli Article does not disclose any structure for verifying the programmed data in each of the plurality of addressed cells with a chunk of stored data. Allen, Tr. 1034, 1191-1192; RX 71 at Fig. 2.
164. The Torelli Article does not disclose any structure for inhibiting programming of correctly verified cells among the plurality of addressed cells. Allen, Tr. 1038, 1192; McGreivy, Tr. 1686; RX 71 at Fig. 2.
165. The Torelli Article does not disclose any structure for further programming and verifying in parallel the plurality of addressed cells and inhibiting the programming of correctly verified cells until all the plurality of addressed cells are verified correctly. McGreivy, Tr. 1686-1691, 1784; RX 71 at Fig. 2.

166. The failure of the Torelli Article to disclose a structure for (1) "temporarily storing a chunk of data for programming a plurality of addressed cells"; (2) "verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data"; (3) "inhibiting further programming of correctly verified cells among the plurality of addressed cells"; and (4) "further programming and verifying in parallel the plurality of addressed cells and inhibiting the programming of correctly verified cells until all the plurality of addressed cells are verified correctly", would preclude an individual of ordinary skill from building the device disclosed in claim 27 of the '338 patent. McGreivy, Tr. 1685, 1787-1788.

Obviousness

167. An individual of ordinary skill in the art of flash memory design and development has a working knowledge of digital logic. McGreivy, Tr. 1650.

168. A working knowledge of digital logic is obtained by someone working probably about two years in the field of integrated circuit design. McGreivy, Tr. 1651.

169. The skill level of an individual with a working knowledge of digital logic is comparable to a bachelor's level degree and some work experience in the field of integrated circuit design. McGreivy, Tr. 1651. Respondents' expert, Dr. Allen, also testified that the level of ordinary skill in the art pertaining to the '338 patent is a bachelor's degree in electrical or computer engineering, an understanding of digital design, computer architecture, and flash EEPROM cell technology, and a few years of work experience in flash EEPROM technology. See RPF 56; Allen, Tr. at 1007.

170. Individuals of ordinary skill in the art of flash memory design and development have an understanding of integrated circuit fabrication, so that they understand the design rules and circuitry provided by wafer manufacturers. McGreivy, Tr. 1650-1653.
171. An individual of ordinary skill in the art of flash memory design and development has knowledge of semiconductor testing. McGreivy, Tr. 1650.
172. An individual of ordinary skill in the art of flash memory design and development understands device specifications. McGreivy, Tr. 1650.
173. The level of ordinary skill in the art of flash memory design and development is the same for both the '338 and '752 patent. McGreivy, Tr. 1650-1651.
174. Samsung introduced as potentially relevant items of prior art excerpts from a 1993 SGS Thomson Data Book which pertained to the following devices: the M193A, M193C, M193D, M206, M293, M490 and M491 (the "M193A Data Book," "M193C Data Book," "M206 Data Book," "M293 Data Book," "M490 Data Book," and "M491 Data Book" respectively). RX 91-100.
175. The M293 Databook does not disclose the function of permanently inhibiting the programming of correctly verified cells. RX 98 at SEC39804-05; McGreivy, Tr. 1691, 1687-1690, 1787-1788.
176. The M206 Data Book does not disclose the function of permanently inhibiting the programming of correctly verified cells. RX 100, at SEC39852; McGreivy, Tr. 1691, 11887-1690, 1787-1788.
177. The M490 and M491 Data Books do not disclose the function of permanently inhibiting the programming of correctly verified cells. RX 99, at SEC39820-21; McGreivy, Tr. 1687-1691, 1787-1788.
178. The M293, M206, M490 and M491 Data Books combined do not disclose the

function of permanently inhibiting the programming of correctly verified cells. McGreivy, Tr. 1691, 1787-1788; CPX 73.

179. The M293 Data Book does not suggest the function of permanently inhibiting the programming of correctly verified cells. RX 98 at SEC39804-05; McGreivy Tr. 1687-1691, 1787-1788.
180. The M206 Data Book does not suggest the function of permanently inhibiting the programming of correctly verified cells. RX 100 at SEC39852; McGreivy, Tr. 1687-1691, 1787-1788.
181. The M490 and M491 Data Books do not suggest the function of permanently inhibiting the programming of correctly verified cells. RX 99 at SEC39820-21; McGreivy, Tr. 1687-1691, 1787-1788.
182. The M293, M206, M490 and M491 Data Books combined do not suggest to an individual of ordinary skill in the art the function of permanently inhibiting the programming of correctly verified cells. McGreivy, Tr. 1687-1691, 1787-1788; RX 98, at SEC39804-05; RX 100, at SEC39852; RX 99, at SEC39820-21.
183. Samsung introduced the SGS Technical Note 152 ("Technical Note 152"), authored by Guido Torelli et. al. in 1982, as a potentially relevant item of prior art. RX 95.
184. Technical Note 152 does not disclose or suggest the function of permanently inhibiting the programming of correctly verified cells. RX 95, at 39736.
185. Samsung introduced the SGS Technical Note 153 ("Technical Note 153"), authored by Guido Torelli et. al. in 1982, as a potentially relevant item of prior art. RX 95.
186. Technical Note 153 does not disclose or suggest the function of permanently inhibiting the programming of correctly verified cells. RX

96, at SEC39754.

187. Samsung introduced the SGS Technical Note 170 ("Technical Note 170"), authored by Guido Torelli et. al. in 1984, as a potentially relevant item of prior art. RX 95.
188. Technical Note 170 does not disclose or suggest the function of permanently inhibiting the programming of correctly verified cells. RX 94, at SEC39774-75.
189. Technical Notes 152, 153 and 170 combined do not disclose the function of permanently inhibiting the programming of correctly verified cells. RX 95, at 39736; RX 96, at SEC39754; RX 94, at SEC39774-75.
190. There is no suggestion in the Torelli Article, M293, M206, M490 and M491 Data books or Technical Notes 152, 153 and 170 that these pieces of art should be combined together to build the invention claimed in claim 27 of the '338 patent. McGreivy, Tr. 1787-1788; RX 71, 94-96, 98-100.
191. The record is devoid of any evidence to suggest that an individual of ordinary skill would have attempted to combine the Torelli Article, M293, M206, M490 and M491 Data books or Technical Notes 152, 153 and 170 to build the invention claimed in claim 27 of the '338 patent. See McGreivy, Tr. 1685, 1787-1788; RX 71, 94-96, 98-100.
192. Dr. Allen, Samsung's validity expert, offered no testimony to suggest that one would know how to combine the Torelli article, SGS data books and SGS technical notes. See Allen, Tr. 1004-1195.
193. In combination, the Torelli Article, M293, M206, M490 and M491 Data books or SGS Technical Notes 152, 153 and 170 do not suggest to an individual of ordinary skill in the art the function of permanently inhibiting the programming of correctly verified cells. McGreivy, Tr. 1685, 1687-1690, 1787-1788; RX 71 at 490 and Fig. 4; CPX 73; RX 98, at

- SEC39804-05; RX 99, at SEC39820-21; RX 100, at SEC39852; RX 95, at 39736; RX 96, at SEC39754; RX 94, at SEC39774-75.
194. In combination, the Torelli Article, M293, M206, M490 and M491 Data books or Technical Notes 152, 153 and 170 do not disclose any structure for inhibiting programming of correctly verified cells among the plurality of addressed cells. Allen, Tr. 1038, 1192; McGreivy, Tr. 1686, 1784; RX 98 at SEC39804-05; RX 99 at SEC39820-21; RX 100 at SEC39852; RX 95 at 39736; RX 96 at SEC39754; RX 94 at SEC39774-75.
195. In combination, the Torelli Article, M293, M206, M490 and M491 Data books or Technical Notes 152, 153 and 170 do not disclose any structure for further programming and verifying in parallel the plurality of addressed cells and inhibiting the programming of correctly verified cells until all the plurality of addressed cells are verified correctly. Allen, Tr. 1038, 1192; McGreivy, Tr. 1686, 1784; RX 98, at SEC39804-05; RX 99, at SEC39820-21; RX 100, at SEC39852; RX 95, at 39736; RX 96, at SEC39754; RX 94, at SEC39774-75.
196. The Torelli Article does not render obvious claim 27 of the '338 patent. See, e.g., McGreivy, Tr. 1685, 1687-1690, 1787-1788; RX 71.
197. The Torelli Article in combination with the SGS data books and technical notes does not render obvious claim 27 of the '338 patent. McGreivy, Tr. 1685, 1687-1690, 1787-1788 RX 71; RX 98 at SEC39804-05; RX 99, at SEC39820-21; RX 100, at SEC39852; RX 95, at 39736; RX 96, at SEC39754; RX 94, at SEC39774-75.
198. The function of permanently inhibiting the programming of correctly verified cells would not be obvious to an individual of ordinary skill in the art. Harari, Tr. 1863-1865, 1867-1868.
199. Toshiba, the original designer of the NAND architecture, did not

- include a permanent inhibit feature in its original 4Mbit memory product. Harari, Tr. 1863-186.
200. The '338 patent has been and will be crucial to SanDisk's success in the mass storage flash memory market. Harari, Tr. 139-140.
201. Intel Corporation, the world's largest commodity flash memory producer, entered into a licensing agreement for all of SanDisk's patents, including the '752 and '338 patents. CX 115; Harari, Tr. 128-120, 281.
202. Intel Corporation acknowledged that a fair and reasonable royalty for SanDisk patents is [[C]] percent in cash and services, with a cap on payments of \$[[C]]per quarter. CX 115 at 8; Harari, Tr. 282-287.
203. In 1994, SanDisk was the worldwide leader in the mass storage flash memory with approximately a 40% market share. Harari, Tr. 138-140.
204. Programming is a very stressful process that reduces the life of an EEPROM device. Harari, Tr. 24-25.
205. Dr. McGreivy believed that a misverify could "easily" occur in the M293 device. McGreivy, Tr. 1796.
206. Dr. McGreivy agreed that because precision was not essential for a TV tuner the inability of the M293 to permanently inhibit the programming of correctly verified cells did not prevent the M293 from providing satisfactory performance. McGreivy, Tr. 1802.
207. There is no explicit reference to the M293 device in the Torelli Article. RX 71.
208. There is no structure disclosed in the Torelli Article that would indicate what was meant by the term bit-per-bit intelligent writing. McGreivy, Tr. 1684-1685.

209. Torelli left it to the reader to infer what bit-per-bit intelligent writing meant. McGreivy, Tr. 1684-1685, 1768-1770.
210. The capacitance of the microprobe used to test the M293 device had no impact on the conclusions of the SanDisk test report because the M293 does not have any structure to terminate the programming of correctly verified cells. Mehrotra, Tr. 1835.
211. As Dr. McGreivy testified at the hearing, the deposition response he gave on July 31, 1996 assumed that the individual of ordinary skill in the art had in his or her possession an M293 part to generate a circuit schematics of the part through reverse engineering. Dr. McGreivy's deposition answer was never meant to be applied to a situation where the individual only had the Torelli Article and SGS Public literature in his or her possession. McGreivy, Tr. 1787-1790.
212. The SGS data book and technical notes disclose only the recommended voltage conditions. RX 94, RX 95, RX 96, RX 97, RX 98, RX 99.
213. The capacitance of the microprobe used to test the M293 device had no impact on the conclusions of the SanDisk test report because the M293 does not have any structure to terminate the programming of correctly verified cells. Mehrotra, Tr. 1835.
214. Claim 27 of the '338 patent does not make any reference to the use of reference cells during a programming operation on the plurality of addressed cells. CX 2 at 26.
215. In the '338 patent, the verification of a cell is a one-time event. A cell can be "correctly verified" only once during a given programming operation on the chunk of addressed cells. Mehrotra, Tr. 253-254; CX 2 at col. 18, line 1 - col. 19, line 16.
216. The specification of the '338 patent clearly states that disclosed

EEprom device disables the programming of all the cells that have been verified. CX 2 at 19.

217. Dr. McGreivy testified that the following portions of the '338 patent specifications formed in part the basis for his opinion that the last element of claim 27 mandated that the device permanently inhibits the programming of correctly verified cells: column 9, lines 5-17; column 18, lines 17-29; and column 19, lines 10-26. McGreivy, Tr. 1693-1696.
218. As Dr. McGreivy testified, terminating the programming of cells upon verification is an essential feature of multistate device. McGreivy, Tr. 1699-1701, 1706.
219. Dr. McGreivy testified that an EProm device will experience greater stress and reduced life if programming of cells is not terminated upon verification. McGreivy, Tr. 1699, 1797-1798.
220. Samsung failed to put forth any type of documentary evidence in support of its claim that termination is not an important feature in a multistate device. Allen, Tr. 999-1195.
221. The purpose of the permanent inhibit feature claimed in claim 27 of the '338 patent is to prevent the application of a programming pulse to a cell that has been verified. McGreivy, Tr. 1699-1701, 1706, 1797-1798.
222. In the '338 patent, the verification of a cell is a one-time event. A cell can be "correctly verified" only once during a given programming operation on the chunk of addressed cells. Mehrotra, Tr. 253-254; CX 2 at 18-19.
223. The specification of the '338 patent clearly states that the disclosed EProm device disables the programming of all the cells that have been verified. CX 2 at 19.

224. Claim 27 of the '338 patent does not make any reference to the use of reference cells during a programming operation on the plurality of addressed cells. CX 2 at 26.
225. As Dr. Harari testified, the permanent inhibit feature of claim 27 would enable a binary device to save power. Harari, Tr. 1864-1865, 1867-1868.
226. Toshiba's NAND products in 1990 and 1991 did not possess a means for terminating programming to correctly verified cells. In 1992, Toshiba's products for the first time contained the termination feature. Harari, Tr. 1867-1868.

The '338 Patent

117. Samsung's flash memory devices are binary devices. CX 56 at 1151 (Samsung IEEE Journal article) ("In program operations, the page buffer latches are first serially loaded with program data: "0" for cells to be programmed and "1" for cells to be inhibited.").
118. Samsung's flash memory devices use a NAND architecture. CX 56 (Samsung IEEE Journal article).
119. Samsung's 4 Mbit, 16 Mbit, 32 Mbit and 64 Mbit flash memory devices operate in substantially the same way with respect to implementation of the '338 patent. Pathak, Tr. 789.

Samsung's Practice of the Preamble of Claim 27

120. Samsung's flash memory devices consist of "an array of addressable semiconductor electrically erasable and programmable memory (EEPROM) cells on an integrated circuit chip" as recited in claim 27 of the '338 patent. Pathak, Tr. 789-790; CX 29 at Bates No. SEC 035132 (Samsung's 1996 data book).
121. Samsung's witnesses did not dispute that Samsung's flash memory devices consist of "an array of addressable semiconductor electrically erasable and programmable memory (EEPROM) cells on an integrated circuit chip" as recited in claim 27 of the '338 patent. Tr. 464-465 (counsel).
122. Samsung's flash memory devices are "of the type having a source, a drain, [and] a control gate" as recited in claim 27 of the '338 patent. Pathak, Tr. 790-791; CX 43, Bates No. SEC 016352 (Samsung product literature).

Samsung's Practice of the "Erase Electrode" Element

123. Samsung's flash memory devices contain "an erase electrode" as that term is used in claim 27 of the '338 patent. Pathak, Tr. 790-791.

124. [[C]

] Pathak, Tr. 792-795; Thomas, Tr. 1579-1580; CX 56
at 1150-51 (Samsung IEEE Journal Article); CX 43C (Samsung product
literature).

125. [[C]

] Pathak, Tr. 790-794.

126. [[C]

] Pathak, Tr. 792-795; Thomas, Tr. 1579-1580; CX 56 at
1150-51 (Samsung IEEE Journal Article); CX 43C (Samsung product
literature).

127. [[C]

] Pathak, Tr. 794-794.

128. [[C]

] Pathak, Tr. 792-795; Thomas, Tr. 1579-1580; CX 56 at 1150-51 (Samsung
IEEE Journal Article); CX 43C (Samsung product literature).

129. [[C]

] Pathak, Tr.

794-794.

130. [[C]

] Pathak, Tr. 792-795;

Thomas, Tr. 1579-1580; CX 56, pp. 1150-51 (Samsung IEEE Journal Article); CX 43C (Samsung product literature).

131. [[C]

] Pathak,

Tr. 795.

Samsung's Practice of the Floating Gate Element

132. Samsung's flash memory devices contain "a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell," as recited in claim 27 of the '338 patent. Pathak, Tr. 795-796; CX 43 (Samsung product literature).

133. Samsung's witnesses did not dispute that Samsung's flash memory devices contain "a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell" as recited in claim 27 of the '338 patent. Thomas, Tr. 1462-1603.

Samsung's Practice of the Increment/Decrement Element

134. Samsung's flash memory devices satisfy the requirement of claim 27 that "a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions" as recited in claim 27 of the '338 patent. Pathak, Tr. 796-798; CX 52 (Samsung's programming algorithm); CX 56 (Samsung

IEEE Journal article).

135. [[C]

] Pathak, Tr. 796-798; CX 52 (Samsung's
programming algorithm); CX 56 (Samsung IEEE Journal article).

136. [[C]

] Choi, Tr. 1351-1352.

137. Neither Mr. Thomas, Samsung's expert on whether SanDisk practices the
'338 patent, nor any other Samsung witness offered any testimony to
rebut Mr. Pathak's conclusion that Samsung's flash memory devices
satisfy the limitation of claim 27 that "a specific memory state is
achieved by increment or decrement of the charge level with successive
applications of programming or erasing voltage conditions." See Thomas,
Tr. 1462-1604.

Samsung's Practice of the Temporary Storage Means

138. Samsung's flash memory devices perform the function of "temporarily
storing a chunk of data for programming a plurality of addressed cells."
Pathak, Tr. 798-805.

139. [[C]

] CX 56 at 1151

(Samsung IEEE Journal article) [[C]

] Pathak, Tr.

803-804 [[C]

] CPX 59.

140. [[C]
] CX 56 at 1151 (Samsung IEEE Journal
article) [[C]
]; CPX 128, line 2.
141. [[C]
] Thomas, Tr. 1584-1585.
142. [[C]
] Pathak, Tr. 799-802; CX 46 (Samsung core
schematics); CX 56 at 1150-51 (Samsung IEEE Journal article); CPX 57C;
CPX 63C (modification of Samsung core schematic).
143. [[C]
] Pathak, Tr. 802-803; CX 2 ('338
Patent), Fig. 5; CX 56 at 1150 (Samsung IEEE Journal article); CPX 59C.
144. [[C]
] Pathak, Tr. 804-805.

Samsung's Practice of the Parallel Programming Means

145. Samsung's flash memory devices perform the function of "programming in parallel the stored chunk of data into the plurality of addressed cells." Pathak, Tr. 805-808.

146. [(C]

] Thomas,

Tr. 1590-1591.

147. [(C]

] Pathak, Tr. 805-808; CX 46C (Samsung core schematic);

CPX 61C.

148. [(C]

] Pathak, Tr. 808; Mehrotra, Tr 337.

149. [(C]

] Pathak, Tr. 808-812; Mehrotra,

Tr. 336.

150. [(C]

]

Pathak, Tr. 808-813; CPX 137-139.

151. [(C]

] Mehrotra, Tr. 336-338; Pathak, Tr.

808-813; CPX 137-139.

Samsung's Practice of the Verification Means

152. Samsung's flash memory devices perform the function of "verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data." Pathak, Tr. 814-81; CPX 60.
153. [[C]
-] Thomas, Tr. 1594-1595; RX 15C at 49 (Expert Report of Mammen Thomas).
154. [[C]
-] Choi, Tr. 1409-1410; CX 56 at 1154 (Samsung IEEE Journal article).
155. [[C]
-] Pathak, Tr. 818-819; CX 48C (Samsung 16 MBit NAND functional block diagram); CPX 60C.
156. [[C]
-] RX 15C at 49 (Expert Report of Mammen Thomas).
157. [[C]
-] Pathak, Tr. 814-820, 829-831, 959-960, 975; RX 205 at 15 (Expert Report of Jagdish Pathak); CX 48C (Samsung 16 MBit functional block diagram); CPX 60C; CPX 127.
158. A flash prom cell must be erased before it can be programmed or reprogrammed. Pathak, Tr. 932-933; CX 2 at col.1, lines 46-54, and col.

19, lines 60-63.

159. [[C]
] Choi, Tr. 1354-1356.

160. The '338 patent discloses that "if each memory cell is to store K states, then at least K-1, or preferably K reference levels need be provided." CX 2 at col. 11, lines 56-58.

161. The '338 patent discloses that in a two-state implementation, only a single reference level is required. CX 2 at col. 11, lines 56-58.

162. The '344 patent, which is incorporated by reference into the '338 patent, discloses that to sense the correct one of K states, only K-1 reference levels and K-1 sense amplifiers are required. CX 3 ('344 Patent) at col. 26, lines 51-55.

163. The '344 patent, which is incorporated by reference into the '338 patent, expressly discloses that a single sense amplifier and a single reference level can be used to differentiate between conduction states "1" (e.g., or programmed) and "0" (e.g., or erased). CX 3 ('344 Patent) at col. 26, lines 55-60.

164. The '344 patent, which is incorporated by reference into the '338 patent, expressly states that Figure 11-E can be implemented using a single sense amplifier. CX 3 ('39644 Patent) at col. 26, lines 8-15.

165. The '344 patent, which is incorporated by reference into the '338 patent, explicitly discloses that "the same principle employed in the circuit of Figure 11-E can be used also with binary storage." CX 3 ('344 Patent) at col. 26, lines 66-67.

Samsung's Practice of the Inhibit Means

166. Samsung's flash memory devices perform the function of "inhibiting further programming of correctly verified cells among the plurality of

addressed cells." Pathak, Tr. 833-835; CPX 62C.

167. [[C]

] Thomas, Tr. 1597.

168. [[C]

] Pathak, Tr. 833-835; CPX 62C.

169. [[C]

] Pathak, Tr. 833-835, 840-841;

CPX 62C, 123, 127.

170. [[C]

] Pathak, Tr. 833-835; CPX 62C.

171. The Samsung flash memory device performs the function of "inhibiting further programming of "correctly verified" cells among the plurality of addressed cells" in an equivalent manner to that disclosed in the '338 patent. Pathak, Tr. 967-969.

172. Dr. McGreivy testified that terminating programming of verified cells will improve the performance of a binary device and prevent it from wearing out a little earlier and is needed in a multi-level device to prevent misprogramming of data. McGreivy, Tr. 1697-1701, 1797-1799.

173. Samsung's devices perform the function of inhibiting further programming of a "correctly verified" cell, until all cells in the chunk have been verified. Pathak, Tr. 842-845; Thomas, Tr. 1597.

174. [[C]

] Pathak, Tr. 840-841

(equating Samsung's page buffer latch with latch 721 disclosed in the patent); CX 56 at 1151, col. 2, lines 21-23); CPX 123 (simplified Samsung verification circuit); CPX 53 (showing Samsung's verification circuit in more detail); CX 56, Fig. 1 (Samsung publication describing the inhibiting scheme); CX 46 C (showing Samsung's most detailed core schematics); Pathak, Tr. 845-846 (equating simplified Samsung circuits to features in core schematics).

175. [[C]

] CPX 60 C

(described at Pathak, Tr. 842-843; CX 56 at 1152, Fig. 5(a); Thomas, Tr. 1519.

176. [[C]

] CX 56 at 1153, col. 1, lines 2-

12; Thomas, Tr. 1119-1120.

177. Flipping the latch 721 disclosed in the '338 patent flips causes 0 volts to be applied to the drain of the disclosed NOR cell. Mehrotra, Tr. 332, 352-353; Pathak, Tr. 967.

178. Although the latch 721 in the '338 patent outputs a logical "1" in the non-verified state while [[C]
] (compare CX 2, Col. 20 with CPX 60-C) these differences are insubstantial given that each signal will inhibit programming in its respective NAND or NOR architecture (see Mehrotra, Tr. 338-339) and that

FIG. 16 of the '338 patent includes an inverter 723 which could be removed to provide the logical output required by Samsung (CX 2).

Samsung's Practice of the Final Means of Claim 27

179. Samsung's flash memory devices perform the function of "further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of "correctly verified" cells until all the plurality of addressed cells are verified correctly." Pathak, Tr. 841-846; CX 46C (Samsung core schematic); CPX 60, 62.

180. [[C]

] Pathak, Tr. 844-845.

181. [[C]

] Pathak, Tr. 841-846; CX 46C (Samsung core schematic); CPX 60, 62.

182. [[C]

] Pathak, Tr. 841-

846; CX 46C (Samsung core schematic); CPX 60, 62.

183. Neither Samsung's Pre-Hearing Statement nor the hearing testimony of Samsung's infringement expert, Mr. Thomas, disputes that if Samsung's

devices fall within the scope of the verify means and the inhibit means,
they also satisfy the final claim 27 means plus function element.

Respondents' Post-Hearing Br.; Thomas, Tr. 1462-1604.

**DECISION ON APPEAL, *SANDISK CORPORATION V.*
MEMOREX PRODUCTS, INC., 415 F.3D 1278, 75USPQ 2D1475
(FED. CIR. 2005)**

granted monopolies like that existing in Tudor England, is not supported by the evidence. As discussed *supra* in note 12, USPTO has issued more than 2 million patents since FY-91, and the requirements that a patentable invention be useful, novel, and non-obvious remain in the statutes, conforming to the constitutional command of the Intellectual Property Clause.

In sum, during the past fourteen fiscal years, USPTO has taken in billions of dollars cumulatively in fees and has provided billions of dollars worth of services, most of which involved issuing more than 2 million patents. USPTO appropriations have increased by a factor of thirteen during that timespan. Congress is, thus, funding USPTO operations, and funding them generously, with money assessed in the form of patent fees, although Congress has not dedicated all of the fees to that particular purpose, choosing instead to spend 4.4 percent of those fees on other priorities. Congress' determination of federal spending priorities and how the patent system fits into national economic development goals is an eminently rational exercise of its power.

Conclusion

Congress is entitled to great deference under the Necessary and Proper Clause when it legislates under its Intellectual Property power. Any intellectual property law Congress passes need only survive the limited scrutiny of the rational basis test as to whether it promotes the progress of science and the useful arts. Plaintiff may well be correct that the current patent fee regime is misguided and creates the wrong incentives, but such policy determinations are for Congress, and not the courts, to make. Plaintiff has not carried his burden of showing that Congress has behaved irrationally.

Having disposed of the case under the Intellectual Property Clause, the court need not reach defendant's Commerce Clause and General Welfare Clause arguments.

Accordingly, plaintiff's motion for summary judgment on his illegal exaction claim is DENIED. Defendant's cross-motion for summary judgment on plaintiff's illegal exaction claim is GRANTED. Plaintiff's motion for class certification, which the court had stayed in an order dated October 7, 2003, is hereby MOOT.

In addition, since the court decides the illegal exaction claim on the merits based on the

broad issue of constitutionality, the question of USPTO pension liabilities is MOOT, and plaintiff's alternative motion for additional discovery is, therefore, DENIED.

The Clerk of the Court shall enter judgment for defendant. No costs.

IT IS SO ORDERED.

SanDisk Corp. v. Memorex Products Inc.

U.S. Court of Appeals
Federal Circuit

Nos. 04-1422, -1610

Decided July 8, 2005

PATENTS

[1] Patent construction — Claims — Broad or narrow (§ 125.1303)

Patent construction — Claims — Process (§ 125.1309)

Language of claims directed to "flash" computer memory system that "includes" array of memory cells which are "partitioned into a plurality of sectors" does not require that every electrically erasable programmable read-only memory cell within device be grouped into sector that is partitioned into "user data" and "overhead data" portions, since claimed method requires "partitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion," since term "includes" is equivalent to "comprising," and thus does not foreclose additional elements that need not satisfy stated claim limitations, since nothing in recitation of these groupings of flash EEPROM cells excludes other configurations of memory cells on physical device that, in some part, practices claimed methods, and since, therefore, nothing in claim language prevents use of flash EEPROMs containing cells that are not grouped into partitioned sectors.

[2] Patent construction — Specification and drawings — In general (§ 125.1101)

Patent construction — Claims — Process (§ 125.1309)

Specification of patent directed to "flash" computer memory system that includes array

of memory cells which are "partitioned into a plurality of sectors" is incompatible with claim construction that requires every electrically erasable programmable read-only memory cell within device to be grouped into sector that is partitioned into "user data" and "overhead data" portions, since specification describes embodiment in which "sector defect map," containing only "overhead" data, is part of flash EEPROM memory, since portions of flash EEPROM memory used in such preferred embodiment would not be partitioned into user data and overhead data portions, and since foregoing claim construction would improperly exclude such embodiment; even if it is assumed that invention is directed only to partitioned sectors, language of asserted claims does not preclude other, unclaimed organizations of flash EEPROM memory cells, and claim terms are not properly limited to preferred embodiment described in specification.

[3] Practice and procedure in Patent and Trademark Office — Prosecution — Disclaimer (§ 110.0925)

Patent construction — Prosecution history estoppel (§ 125.09)

Patentee, during prosecution of application for patent directed to "flash" computer memory system that includes array of memory cells which are "partitioned into a plurality of sectors," did not clearly and unmistakably disclaim any method or device in which electrically erasable programmable read-only memory cells are not grouped into partitioned sectors, since patentee's description of "each sector" as having both "user data" and "overhead data," considered in context, can be read as referring to "each sector" subject to claimed method, and no more, since arguments explicating claimed invention did not purport to exclude other configurations of flash EEPROM memory cells, and since patentee's statement that it sought to have claimed invention emulate disk drive memory configuration does not compel conclusion that patentee required every flash EEPROM cell to be grouped into partitioned sectors.

[4] Infringement — Defenses — Estoppel; laches (§ 120.1103)

JUDICIAL PRACTICE AND PROCEDURE

Procedure — Defenses — Estoppel (§ 410.1805)

Patent infringement plaintiff is not judicially estopped from arguing broad claim construction asserted in present case, since analysis underlying claim construction in prior litigation did not extend to issue presently at bar, since plaintiff therefore did not advance claim construction in prior litigation that was "clearly inconsistent" with construction asserted in present case, and federal district court in prior case cannot be said to have adopted such position at plaintiff's urging, and since equitable principles do not favor applying judicial estoppel to prevent claim construction arguments from evolving after preliminary injunction stage, as they did in present case.

[5] Procedure — Judicial review — Standard of review — In general (§ 410.4607.01)

Federal district court's application of its local rules are reviewed for determination of whether court's decision was clearly unreasonable, arbitrary, or fanciful, or based on erroneous conclusion of law, whether court's findings were clearly erroneous, or whether record contains no evidence upon which court rationally could have based its decision; in present case, district court hearing patent infringement action did not abuse its discretion by refusing to consider defendant's arguments concerning claim construction and infringement that were presented after relevant cut-off dates under court's relevant local rules.

Particular patents — Electrical — EEPROM memory system

5,602,987, Harari, Norman, and Mehrotra, flash EEPROM system, summary judgment of noninfringement vacated.

Appeal from the U.S. District Court for the Northern District of California, Walker, C.J.M.
Action by SanDisk Corp. against Memorex Products Inc. (formerly d/b/a Memtec Proda

ucts Inc.), Pretec Electronics Corp., Power Quotient International Co. Ltd., and Ritek Corp. for patent infringement. Plaintiff appeals from summary judgment of noninfringement. Vacated and remanded.

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Ronald C. Finley, Daniel S. Mount, Alfredo A. Bismonte, and Justin T. Beck, of Mount & Stoelker, San Jose, Calif., for defendant-appellee Pretec Electronics Corp.

Alan D. Smith and Charles H. Sanders, of Fish & Richardson, Boston, Mass., for defendant-appellee Ritek Corp.

Before Rader, Gajarsa, and Dyk, circuit judges.

Gajarsa, J.

SanDisk appeals the district court's judgment of no infringement in favor of Memorex, Pretec, and Ritek. The district court granted summary judgment that various Flash memory devices made by these defendants did not infringe independent claims 1 or 10—or various claims depending therefrom—in SanDisk's U.S. Patent No. 5,602,987 to Flash EEPROM systems. The trial court ruled that the claims at bar did not contemplate or allow for a Flash memory system in which some EEPROM memory cells are grouped into sectors that are not partitioned into user and overhead data portions. As the record showed that the defendants' products contained sectors of memory cells lacking such partitions, the trial court determined that these defendants could not infringe. We conclude that the trial court misread the claims at issue, and erred in finding a prosecution disclaimer in support of its reading. We further reject the contention that judicial estoppel forecloses SanDisk's claim construction arguments on appeal. Thus, we vacate the judgment and remand for further proceedings.

I.

A.

SanDisk Corp. ("SanDisk") owns U.S. Patent No. 5,602,987 to Flash EEPROM systems ("the '987 patent").¹ The '987 patent is sued on February 11, 1997, and describes methods for using EEPROMs as non-volatile solid state computer memory. A non-volatile memory retains its contents even after power is shut off. This "flash memory" has many applications, including the memory used in digital cameras, PDAs, memory sticks or MP3 players.

Flash EEPROMs can sustain only a limited number of writes and erases before they fail. The '987 system and methods include innovations directed at improving flash memory performance and extending EEPROM life. The patent focuses, in particular, on improving the memory system architecture over the prior art. The memory architecture generally concerns how the memory system solves the problem of storing or retrieving specific information from the memory cells. See '987 patent, col. 5, ll. 4-21. If the architecture can be designed to minimize the number of times each EEPROM memory cell is erased and rewritten, then that solution can extend the useful life of the integrated circuit. If the architecture allows for faster operations, then the EEPROM performance will improve.

The '987 patent addresses these issues in at least two ways relevant to this appeal. First, it introduces a multi-sector erase function. In earlier systems either every memory cell in an EEPROM would be written or erased in one operation, or only a single "sector" could be erased in one operation. See '987 patent, col. 4, ll. 46-63. Where not all the information was to be erased, systems that operated only on the entire chip had to read that information out, store it in a temporary location (typically a different, volatile memory or RAM), erase the entire chip, and then write the information back into the EEPROM memory. *Id.* The other approach, operating sequentially on individual sectors, proved time-consuming.

The '987 patent describes a different way of organizing the memory storage, and in particular arranges memory cells into "sectors" akin to the physical "sectors" used for storage

¹ Electrically erasable programmable read only memory (EEPROM).

on magnetic disk drives. The '987 patent allows the operator to select multiple sectors for simultaneous erase. The defining feature of the "sector" of memory cells is that all cells within the sector are erased together. See '987 patent, col. 1, ll. 65-66 ("[A]n array of Flash EEPROM cells on a chip is organized into sectors such that all cells within each sector are erasable at once."); *id.* at col. 5, ll. 9-11 ("The memory in each Flash EEPROM chip is partitioned into sectors where all memory cells within a sector are erasable together."). Put differently, the "sector" is the "basic unit of erase." The '987 patent illustrates this architecture, as implemented on a single EEPROM or integrated circuit (chip), in Fig. 3A.

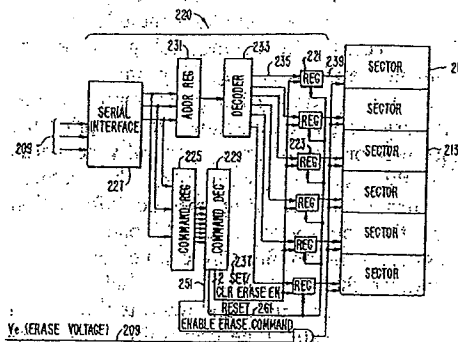
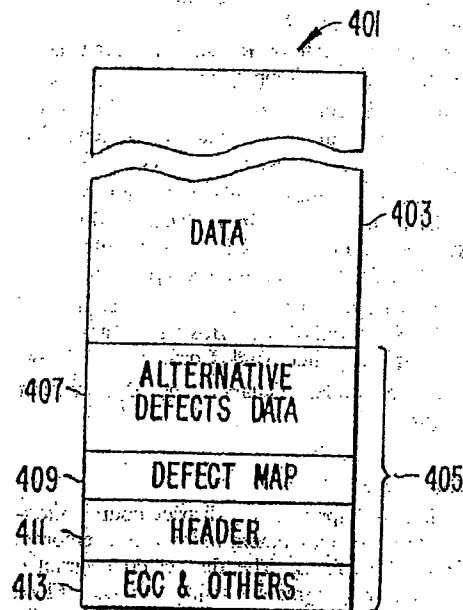


FIG. 3A

Although the block diagram in Fig. 3A illustrates the description of multiple sectors on a single chip, the multi-sector erase feature is not limited to individual EEPROMs. As the '987 patent notes, "the selected sectors [for erase] may be confined to one EEPROM chip or be distributed among several chips in a system. The sectors that were selected will all be erased together." '987 patent, col. 5, ll. 16-19. Because this allows more intelligent use of the memory, avoiding needless erases, it improves performance and extends the operational life of the EEPROMs. As the patent explains, "[t]his is faster and more efficient than prior art schemes where all the sectors must be erased every time or only one sector at a time can be erased. The invention further allows any combination of sectors selected for erase to be deselected and prevented from further erasing during the erase operation." '987 patent, col. 2, ll. 4-7.

Second, the architecture described in the '987 patent further requires "partitioning" the

"sectors" into at least two components—one for "user data," and a second for "overhead." "User data" means the information that the processor stores or on which it operates. "Overhead data" refers to administrative information used by the memory controller, such as data address information (typically the information included in a header), memory cell defect maps, error correction code, and so on. The memory allocation in a "typical" sector is illustrated in Fig. 5:



SECTOR PARTITION

FIG. 5.

SanDisk argues that this feature "improves the reliability of Flash EEPROM memory systems." The written description explains,

The memory architecture has a typical sector 401 organized into a data portion 403 and a spare (or shadow) portion 405. The data portion 403 is memory space available to the user. The spare portion 405 is further organized into an alternative defects data area 407, a defect map area 409, a header area 411 and an ECC and others area 413. These areas contain information that could be used by the controller to handle the data

fects and other overhead information such as headers and ECC.
 '987 patent, col. 8, ll. 43-50.

B.

In 1998 SanDisk accused Lexar Media Inc. ("Lexar") of infringing claims 1 and 10 of the '987 patent. The action was assigned to Judge Breyer in the Northern District of California. On March 4, 1999, Judge Breyer issued a claim construction order interpreting the "user data and overhead data portions." He expressly limited the order to "those terms and issue[s] discussed by both parties in their memoranda and at the claim construction hearing." *SanDisk Corp. v. Lexar Media, Inc.*, No. C 98-01115 CRB, 1999 WL 129512, at *2 (N.D. Cal. Mar. 4, 1999).

With that caveat, Judge Breyer ruled that the partitioning and user data / overhead data limitations meant that

Each non-volatile memory sector must have at least one user data portion and one overhead data portion, but is not limited to only one data user portion and only one overhead data portion.

Id. at *3. SanDisk eventually obtained a judgment of infringement against Lexar.

C.

In October 2001, SanDisk sued four Flash memory system manufacturers: Memorex Products, Inc. ("Memorex"); Pretec Electronics Corp. ("Pretec"); Ritek Corp. ("Ritek"); and Power Quotient International Co., Ltd., for infringing the '987 patent, claims 1 and 10 (and various dependent claims). In due course Power Quotient was dismissed from suit.

SanDisk sought a preliminary injunction based on Judge Breyer's claim construction. The defendants opposed, and the trial court denied the motion. In assessing the partitioning limitation, the trial court heavily relied on the prosecution history:

SanDisk specifically limited its claim to include only those devices in which each sector within a memory cell array contains both overhead and user data. SanDisk cannot now argue that only some of the sectors of a memory cell array need to contain user data and overhead data.

On September 30, 2003, the district court construed claims 1 and 10 to require that ev-

ery cell in the memory device be grouped into a sector, and every sector be partitioned into user and overhead data portions. *See SanDisk Corp. v. Memorex Prods., Inc.*, No. C-01-4063 VRW, slip. op. at 34 (N.D. Cal. Apr. 20, 2004) ("Pretec SJ Order") ("[T]he court's claim construction requires all sectors within the memory array to be partitioned.").

Although the trial court's claim construction considered the claim language and the written description, the court relied primarily on a finding of prosecution disclaimer. *Id.* at 28 ("[T]he court finds that SanDisk clearly and unmistakably disclaimed coverage of systems in which only some of the sectors in the array were partitioned into at least user data and overhead portions."); *see also id.* at 16-29.

With that claim construction the trial court granted Ritek summary judgment of non-infringement, because Ritek had presented evidence that their products include some sectors that are not partitioned.

Pretec and Memorex moved for summary judgment on the same ground. The court granted Pretec's motion on April 20, 2004, and Memorex's motion on May 13, 2004, after each party supplemented the record with evidence about their devices.

The trial court entered judgment of no infringement. SanDisk timely appealed. Ritek and Pretec separately oppose. Memorex joins in Pretec's opposition. Pretec adopts Ritek's arguments in opposition by reference, but did not file a separate joinder. The court has jurisdiction under 28 U.S.C. § 1295(a)(1) (2000).

II.

The court reviews *de novo* the trial court's summary judgment of no infringement. *Hilgraeve Corp. v. McAfee Assocs., Inc.*, 224 F.3d 1349, 1352 [55 USPQ2d 1656] (Fed. Cir. 2000). Summary judgment is proper only if the movants are entitled to judgment as a matter of law, and no genuine issue of material fact requires a determination by a fact-finder. *See Fed. R. Civ. P. 56(c); Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 250 (1986). In this case there are no disputed material facts at issue. The judgment turns solely on claim construction, which the court reviews *de novo*. *See Cybor Corp. v. FAS Techs., Inc.*, 138 F.3d 1448, 1456 [46 USPQ2d 1169] (Fed. Cir. 1998) (en banc).

A.

The court's claim construction ascribes claim terms the meaning they would be given by persons of ordinary skill in the relevant art at the time of the invention. See 35 U.S.C. § 112; *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1116 [72 USPQ2d 1001] (Fed. Cir. 2004). Claim construction begins with the language of the asserted claims. See *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 [39 USPQ2d 1573] (Fed. Cir. 1996). The relevant claim language in this case appears identically in independent claims 1 and 10. It provides,

A method of operating a computer system including a processor and a memory system, wherein the memory system includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit, comprising:

providing said memory array and a memory controller within a card that is removably connectable to the computer system, said controller being connectable to said processor for controlling operation of the array when the card is connected to the computer system,

partitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion.

'987 patent, col. 16, ll. 24-37 (claim 1, *emphasizes added*); see also *id.* at col. 17, ll. 30-44 (claim 10). Although SanDisk also asserted claims 2, 5, 6, 12, and 15 of the '987 patent, each depends from claim 1 or 10 and incorporates the forgoing limitations in relevant part. The parties do not dispute, and the trial court correctly noted, that the preamble recited above is limiting.²

Reviewing the partitioning requirement, the trial court concluded that claim 1 and claim 10 require every Flash EEPROM memory cell within an actual device to be grouped into a sector that is partitioned into user and over-

head data portions. SanDisk argues that this construction misreads the plain language of the claim. The argument proceeds on two levels. First, by its plain language, claims 1 and 10 require only that the claimed memory system contain some memory cells, grouped into sectors, partitioned into user and overhead data portions. Nothing in the claims precludes additional memory cell configurations, which need not contain such partitioned sectors. Second, claims 1 and 10 are self-evidently drawn to claimed methods. It is fully consistent with practicing the claimed invention to make additional, unclaimed use of Flash EEPROM memory cells, so long as each limitation is satisfied. We agree.

[1] The invention is claimed using non-restrictive terminology. The memory system "includes" an array of "non-volatile floating gate memory cells" which are "partitioned into a plurality of sectors." The claimed method requires "partitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion." As a patent law term of art, "includes" means "comprising." See *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1344-45 [65 USPQ2d 1385] (Fed. Cir. 2003); *Hewlett-Packard Co. v. Repeat-O-Type Stencil Mfg. Corp., Inc.*, 123 F.3d 1445, 1451 [43 USPQ2d 1650] (Fed. Cir. 1997). Neither includes, nor comprising, forecloses additional elements that need not satisfy the stated claim limitations. Nor does the choice of articles—"an array" of memory cells, "a plurality of sectors," "said array of memory cells," "the memory cells," or "the individual sectors"—compel a different conclusion. These groupings of Flash EEPROM memory cells provide an antecedent basis for various steps of the claimed method, but nothing in their recitation excludes other configurations of memory cells on a physical device that, in some part, practices the claimed methods. Thus, nothing in the language of claims 1 or 10 prevents the use of Flash EEPROMs containing cells that are not grouped into partitioned sectors.

B.

SanDisk further argues that the '987 patent specification is inconsistent with the trial court's claim construction because, among other reasons, it excludes at least two preferred embodiments: one involving storing a sector defect map in Flash EEPROM memory cells, and another involving using Flash EEPROM

² That is, because "when read in the context of the entire claim" the preamble "recites limitations of the claim . . . or . . . is necessary to give life, meaning, and vitality" to claims 1 and 10, the trial court properly treated the language as limiting. *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 [51 USPQ2d 1161] (Fed. Cir. 1999).

rom cells as a write memory cache. As explained below, the court need only consider the sector defect map to conclude that SanDisk is correct.

[2] The court must always read the claims in view of the full specification. *See Vitronics*, 90 F.3d at 1582. A claim construction that excludes a preferred embodiment, moreover, "is rarely, if ever, correct." *Vitronics*, 90 F.3d at 1583; see also *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 865 [73 USPQ2d 1011] (Fed. Cir. 2004). The '987 patent specification describes an embodiment involving a sector defect map, which, in brief, contains information mapping defective memory sectors into good ones. *See* '987 patent, col. 11, ll. 57-60. Although the defect map may be stored in spare, defect-free portions of the affected sector, at some point there will be too many defects to keep the defect map in that location. "Thus, it is preferable in another embodiment to locate the sector map in another memory maintained by the controller. The memory may be located in the controller hardware or be part of the Flash EEPROM memory." '987 patent, col. 11, l. 65—col. 12, l. 1 (emphasis added). SanDisk argues that because the sector defect map would contain only overhead data, the portions of the Flash EEPROM memory used in the preferred embodiment would not be partitioned into user data and overhead data portions as required by according claims 1 or 10. As the district court's claim construction would foreclose that possibility, the claim construction must be wrong.

The trial court rejected this argument. It ruled, instead,

The fact that the sector defect map contains only overhead data does not prove that the embodiment contemplates sectors with only overhead data. Although the sector defect map is composed entirely of overhead data, the court finds that the sector defect map is located entirely within the overhead portion of a single sector.

We find this reasoning misplaced.

In its brief to this court Ritek concedes that the sector defect map could be located in "a part of memory outside the array of sectors partitioned into a user data and overhead portions, i.e., in an unsectored part of the memory." Ritek Br. at 43-44. If Ritek is correct, then the trial court's claim construction must be wrong. The claims must allow, instead, for Flash EEPROM memory cells that are

not sectored, or not partitioned, according to the claimed methods. But since Ritek concedes this point, and both Pretec and Memorex join Ritek's argument, there is no dispute left for the court to resolve. In sum, the trial court's speculative treatment of the preferred embodiment is unsupported by the patent specification, not grounded in the record, and contrary to the reading suggested by all parties. We conclude that SanDisk is correct in faulting the trial court's claim construction.

Ritek contends that the only sectors described in the '987 patent specification are partitioned as illustrated in Fig. 5. Thus, Ritek concludes, the invention is directed only to partitioned sectors. We find this reasoning misplaced for at least two reasons. First, as noted above the language of claims 1 and 10 does not preclude other, unclaimed organizations of Flash EEPROM memory cells. Thus, even if the court concluded that Fig. 5 shows the only partitioning consistent with the claimed methods that would not preclude use of other organizations in the memory system. Second, it is axiomatic that without more the court will not limit claim terms to a preferred embodiment described in the specification. *Lairam Corp. v. Cambridge Wire Cloth Co.*, 863 F.2d 855, 865 [9 USPQ2d 1289] (Fed. Cir. 1988) ("References to a preferred embodiment, such as those often present in a specification, are not claim limitations."). The '987 patent specification plainly describes the sector partitioning illustrated at Fig. 5 as a "typical" sector organization. *See* '987 patent, col. 8, ll. 43-45. It is a preferred embodiment of the sector organization claimed in the claim 1 and 10 methods. In short, Ritek's argument is misplaced. The specification does not contradict the plain meaning of claims 1 and 10.

C.

The prosecution history does not compel a contrary result. The court must always consult the prosecution history, when offered in evidence, to determine if the inventor surrendered disputed claim coverage. *See Medrad, Inc. v. MRF Devices Corp.*, 401 F.3d 1313, 1319 [74 USPQ2d 1184] (Fed. Cir. 2005) ("We cannot look at the ordinary meaning of the term ... in a vacuum. Rather, we must look at the ordinary meaning in the context of the written description and the prosecution history.").

After consulting the prosecution history, the trial court ruled that SanDisk disclaimed any

method or device in which Flash EEPROM memory cells were not grouped into partitioned sectors. Ritek urges the court to affirm this analysis. SanDisk, however, maintains that the trial court erred in this conclusion. Instead, SanDisk argues, nothing in the prosecution history provides a clear and unmistakable disclaimer as found by the district court. On reviewing the relevant arguments to the examiner, we agree with SanDisk.

1.

When the patentee makes clear and unmistakable prosecution arguments limiting the meaning of a claim term in order to overcome a rejection, the courts limit the relevant claim term to exclude the disclaimed matter. See *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324 [67 USPQ2d 1321] (Fed. Cir. 2003) (“[W]here the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender.”); *Standard Oil Co. v. Am. Cyanamid Co.*, 774 F.2d 448, 452 [227 USPQ 293] (Fed. Cir. 1985) (“[T]he prosecution history (or file wrapper) limits the interpretation of claims so as to exclude any interpretation that may have been disclaimed or disavowed during prosecution in order to obtain claim allowance.”).

As this court has explained,

The doctrine of prosecution disclaimer [precludes] . . . patentees from recapturing through claim interpretation specific meanings disclaimed during prosecution. See *Schriber-Schroth Co. v. Cleveland Trust Co.*, 311 U.S. 211, 220-21 (1940). (“It is a rule of patent construction consistently observed that a claim in a patent as allowed must be read and interpreted with reference to claims that have been cancelled or rejected, and the claims allowed cannot by construction be read to cover what was thus eliminated from the patent.”); *Crawford v. Heysinger*, 123 U.S. 589, 602-04 (1887); *Goodyear Dental Vulcanite Co. v. Davis*, 102 U.S. 222, 227 (1880); cf. *Graham v. John Deere Co.*, 383 U.S. 1, 33 [148 USPQ 459] (1966) (ruling, in addressing the invalidity of the patents in suit, that “claims that have been narrowed in order to obtain the issuance of a patent by distinguishing the prior art cannot be sustained to cover that

which was previously by limitation eliminated from the patent”).

As a basic principle of claim interpretation, prosecution disclaimer promotes the public notice function of the intrinsic evidence and protects the public's reliance on definitive statements made during prosecution. See *Digital Biometrics, Inc. v. Identix, Inc.*, 149 F.3d 1335, 1347 [47 USPQ2d 1418] (Fed. Cir. 1998).

Omega, 334 F.3d at 1323-24.

An ambiguous disclaimer, however, does not advance the patent's notice function or justify public reliance, and the court will not use it to limit a claim term's ordinary meaning. See *id.* at 1324 (collecting cases). There is no “clear and unmistakable” disclaimer if a prosecution argument is subject to more than one reasonable interpretation, one of which is consistent with a proffered meaning of the disputed term. See *Golight, Inc. v. Wal-Mart Stores, Inc.*, 355 F.3d 1327, 1332 [69 USPQ2d 1481] (Fed. Cir. 2004) (finding no disclaimer because “the statements in the prosecution history are subject to multiple reasonable interpretations, they do not constitute a clear and unmistakable departure from the ordinary meaning of the term [at issue]”); *Cordis Corp. v. Medtronic AVE, Inc.*, 339 F.3d 1352, 1359 [67 USPQ2d 1876] (Fed. Cir. 2003) (concluding that a statement made during prosecution “is amenable to multiple reasonable interpretations and it therefore does not constitute a clear and unmistakable surrender”). The question, therefore, is whether any of SanDisk's prosecution arguments to the examiner have no reasonable interpretation other than to disavow any memory system in which Flash EEPROM memory cells are not grouped into partitioned sectors.

2.

In this case the relevant prosecution argument responded to an obviousness rejection. The '987 patent issued from application Ser. No. 174,768 (“the '768 application”). On December 7, 1995, the examiner rejected original claims 79 (which issued as claim 1) and 85 (which issued as claim 10) in the '768 application as obvious under Burke in view of Yorumoto. The examiner explained that Burke—an Australian patent, No. AU-B-22536/83—taught a memory system including

"an array of cells which are inherently partitioned into a plurality of sectors because Burke's array is to 'emulate' a magnetic disk which has sectors." As the examiner explained, Yorimoto—European patent application No. 86114972.2, Pub. No. 0 220 718—"teaches partitioning the cells with a sector into portions, each portion is for storing a specific type of information." Rejecting claim 85 (issued claim 10), the examiner concluded,

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use Yorimoto's memory (of EEPROM type) and Yorimoto's memory cells partitioning in place of Burke's memory.

The artisan would have been motivated to use Yorimoto's EEPROM in the place of Burke's memory because Yorimoto's EEPROM can be partitioned into sectors and Burke's emulation inherently suggests that the emulating memory should be able to emulate the sectors of Burke's magnetic disk.

SanDisk argued that the examiner was mistaken. In particular, SanDisk explained:

The memory cell array is divided into sectors, with the cells within each sector being erasable together as a unit. Stored in each sector is a sectors [sic] worth of user data and some overhead information (a header) about the sector and/or about the user data stored in the sector.

(quoted at Pretec SJ Order, slip. op. at 25). Relying heavily on SanDisk's description of "each sector", the trial court concluded that SanDisk was referring to every sector on the '987 patent EEPROMs. *Id.* at 26. Ritek contends that the trial court's analysis was correct, and with this language SanDisk disclaimed its current claim construction. We disagree, and find no clear and unmistakable disclaimer in this passage.

[3] The trial court's and Ritek's reasoning assumes its conclusion. The quoted passage begins with the proviso that "The claims are directed to a flash EEPROM system[.]" If, when viewed in context, SanDisk used this passage to describe the memory cell array—and, in particular, the claimed sector organization subject to the methods in original claims 79 and 85—then there is no prior reason why that memory cell array or the discussion of it should be presumed to exhaust every cell on

every EEPROM in the "memory system" recited in the claim preambles. Given the open language in the claims, there is no reason for the court to read the prosecution argument with such a presumption in mind. Put differently, the reference to "each sector" means "each sector" subject to the claimed method, and no more. In short, SanDisk's reading of this prosecution argument is at least reasonable. Thus, focusing on this passage alone, there is no "clear and unmistakable surrender" within the meaning of *Golight*.

The trial court further reasoned that because SanDisk sought to emulate a disk drive with the claimed memory system, it followed that SanDisk intended to group every Flash EEPROM memory cell into a partitioned sector. The trial court focused on the following prosecution argument, responding to the obviousness rejection of original claim 79:

The claims in this application each define more than the desire to make a semiconductor memory system look on the host system side of the memory controller to be a disk drive. They define a way of configuring and using a semiconductor memory on the memory side of the controller in a way similar to a disk drive. Claim 79 defines a flash EEPROM system with an array that is divided into sectors of cells that are erasable together as a unit. This is not new by itself but is a particular type of memory to be used to emulate a disk drive. None of the . . . cited references suggest use of such a type of memory. The only mention of an EEPROM system is by Yorimoto et al, but their embodiments appear to be generically described for use with either an EEPROM or a battery backed volatile RAM. Nothing is said by Yorimoto et al. of a flash EEPROM system that is operated with sectors of cells that are erasable together as a unit. It is the use of this type of memory that allows the memory itself to be operated very similarly to that of a disk drive, with individual sectors that store both user data and overhead data (a header for the sector). It is the operation of the flash EEPROM memory by the memory controller with the sectored and partitioned characteristics of a disk drive memory that is novel and non-obvious.

Ritek contends that the trial court correctly read this passage to disclaim the claim construction set forth above. Again, we disagree.

First, as with the last passage, this argument is directed to explicating the claimed invention. It does not purport to exclude from the "memory system" other configurations of Flash EEprom memory cells. Even though SanDisk identifies the novel invention as "operation of the flash EEPROM memory by the memory controller with the sectorized and partitioned characteristics of a disk drive memory," that statement goes to the claimed memory organization.

Second, the fact that with the claimed invention SanDisk sought to emulate a disk drive memory storage configuration does not compel the conclusion that SanDisk required every Flash EEprom memory cell in the "memory system" recited in the claims to be grouped into partitioned sectors. The trial court's reasoning, in short, relies on a false analogy. Though every memory cell on a disk drive might have a physical location in a partitioned sector, it does not follow that to "emulate" that function every memory cell in a Flash EEprom array must also be so grouped. To the contrary, the organization of memory cells in the Flash EEprom is physically limited only by the requirement of a simultaneous erase by sector; in other respects, the cells are grouped into sectors by a logical allocation. Thus, while physical organization of memory on a disk drive might require every memory cell to be placed in a partitioned sector, the physical organization of memory cells on an EEprom does not.

The prosecution history as a whole confirms this point. In an earlier passage, SanDisk argued:

The claimed memory system looks to the host computer as if it was a disk drive system, similar to the goal stated in the cited Burke patent. But a significant difference is the claimed operation of the flash EEPROM array with many incidents of a disk system. It is divided into sectors that are operated as a unit, including overhead data (a header) as well as user data, and, in some of the claims, the overhead data is read from an addressed sector before user data is written into that sector.

(emphases added). The passage focuses on the claimed operation of the flash EEprom memory cell array, the subject of claims 1 and 10; it does not address itself to unclaimed uses of the memory cells. Moreover, according to SanDisk, that particular EEprom configuration

was not obvious from combining Burke, which emulated a disk drive, and Yorimoto, which claimed an EEprom array:

This is quite different from the way that semiconductor memory arrays are usually operated. . . . The present claims . . . define a disk like approach to semiconductor memory operation. The fact that the system of the Burke patent may look to the host system as a disk memory system does not mean that its array is operated in sectors, with headers, etc., as claimed. . . .

[T]he flash EEPROM system employed in the present invention, unlike typical RAMs, do have memory operations that can benefit from auxiliary information. The provision for making such information available in a header of each sector in the context of a solid state memory is part of the present invention.

An underlying assumption made throughout the Examiner's Action is that it is inherent in the system of the cited Burke reference to operate its volatile RAM array with sectors, and thus obvious to include overhead data (headers) in individual sectors. This premise, and thus all the rejections based upon it, is respectfully submitted to be incorrect. Contrary to the position taken in the Examiner's Action, it is submitted that the fact that Burke's system looks to the host system as a disk drive memory does not compel this conclusion. The alleged inherent Burke disclosure upon which nearly all the grounds of rejection are based does not exist.

In other words, it was novel to organize the cells into partitioned sectors for purposes of the claim, but the claimed purpose of emulating a disk drive did not compel sorting every memory cell—even those not subject to the claimed method—in that fashion.

In sum, we conclude that SanDisk did not unmistakably surrender the grouping of Flash EEprom memory cells into non-partitioned sectors. The prosecution history is consistent with the plain meaning of claims 1 and 10, and does not compel the trial court's contrary reading.

D.

Ritek argues that equity requires judicially estopping SanDisk from arguing the claim

construction discussed above because SanDisk argued, in earlier litigation and on preliminary injunction in this action, that claims 1 and 10 required every memory cell in the Flash EEPROM memory to be grouped into partitioned sectors.³ Thus, according to Ritek, "SanDisk should be estopped from playing fast and loose with the courts by changing the meaning of its patent claims simply because its interests have changed now that it knows how Ritek's products work." Ritek Br. at 25-26. We find this argument misplaced.

Judicial estoppel is an equitable doctrine that prevents a litigant from "perverting" the judicial process by, after urging and prevailing on a particular position in one litigation, urging a contrary position in a subsequent proceeding—or at a later phase of the same proceeding—against one who relied on the earlier position. See *Hamilton v. State Farm Fire & Cas. Co.*, 270 F.3d 778, 782 (9th Cir. 2001); *Data Gen. Corp. v. Johnson*, 78 F.3d 1556, 1565 (Fed. Cir. 1996). It is within the trial court's discretion to invoke judicial estoppel and preclude an argument. *Id.* Here, the trial court did not apply the doctrine and the appellees ask this court, in its appellate jurisdiction, to find an estoppel.

As the Supreme Court recently explained,

Where a party assumes a certain position in a legal proceeding, and succeeds in maintaining that position, he may not thereafter, simply because his interests have changed, assume a contrary position, especially if it be to the prejudice of the party who has acquiesced in the position formerly taken by him.

New Hampshire v. Maine, 532 U.S. 742, 749 (2001) (cit. omitted); see also *id.* at 749-50 (collecting cases). In *New Hampshire*, the Supreme Court identified several factors guiding the decision to apply judicial estoppel: (1) the party's later position must be "clearly inconsistent" with the earlier position; (2) the party must have succeeded in persuading a court to adopt the earlier position in the earlier proceeding; and (3) the courts consider "whether the party seeking to assert an inconsistent position would derive an unfair advantage or impose an unfair detriment on the opposing

party if not estopped." *Id.* at 751. These factors, while not exclusive, must guide the court's application of its equitable powers. *Id.*

[4] Ritek's judicial estoppel argument loses force when tested against these criteria. First, in the *Lexar* litigation, SanDisk never advanced a claim construction that was "clearly inconsistent" with the partitioning analysis discussed above. The trial court in *Lexar* therefore cannot be said to have adopted such a position at SanDisk's urging. The district court here recognized that very point in its summary judgment and claim construction order. As it noted, "SanDisk's argument [for the analysis set forth above] draws some strength from the limited nature of the *Lexar* court's construction. The *Lexar* court did not explicitly construe the broader phrase from the patent [citing partitioning step]. The *Lexar* court limited its construction to the 'user data and overhead data portions' of claims 1 and 10." As SanDisk observes, the issue before Judge Breyer in *Lexar* was whether the sectors subject to the claim 1 and claim 10 methods were limited to a single user and data portion, or whether those sectors could be further partitioned. In short, *Lexar* involved a different dispute concerning the claim terms.

Second, SanDisk's arguments at preliminary injunction in this action were no more "clearly inconsistent" than the arguments in *Lexar*. In support of preliminary injunction, SanDisk argued that the preamble to claims 1 and 10 required "partitioning the array of non-volatile memory sector cells into at least a user data region and an overhead data region." SanDisk further argued, invoking the *Lexar* construction of "partitioned", that the claim required "each non-volatile" memory sector must have at least one user data portion and one overhead data portion, but is not limited to only one data user portion and only one overhead data portion."

As explained above, these arguments are directed to the claimed method, and the claims do not preclude additional memory cells that are not organized according to that method. Moreover, at preliminary injunction SanDisk plainly urged the *Lexar* claim construction, and that analysis did not extend to the issue at bar. Thus, there was no inconsistency between the arguments at preliminary injunction, and the disputed construction now on appeal. In sum, the factual premise of Ritek's argument

³ Pretec adopted Ritek's arguments by reference. Memorex filed a joinder in Pretec's brief. Each appellee thus relies on Ritek's judicial estoppel argument.

is misplaced. There is no basis for judicial estoppel here.

Moreover, the equities do not favor applying judicial estoppel to prevent claim construction arguments from evolving after preliminary injunction. The law provides, for example, that the trial court is free to revisit an initial claim construction adopted for preliminary injunction, recognizing that a preliminary construction made without full development of the record or issues should be open to revision. See *Gillette Co. v. Energizer Holdings, Inc.*, 405 F.3d 1367, 1375 [74 USPQ2d 1586] (Fed. Cir. 2005). After discovery the court expects the parties to refine the disputed issues and learn more about the claim terms and technology, at which point a more accurate claim construction can be attempted. That is precisely what happened here. If, as it appears, SanDisk initially thought every memory cell on the accused Ritek products came within the claimed method, then there was no occasion to consider whether other, non-sectored or non-partitioned sectors of memory cells could be used in conjunction with claims 1 or 10. Thus, the present dispute only became an issue after further discovery. Applying judicial estoppel here would subvert the useful function of pre-trial discovery and motion practice in focusing issues for trial. In sum, judicial estoppel does not prevent SanDisk from maintaining its current claim construction arguments.

E.

The parties further dispute the meaning of "array" as used in claims 1 and 10. The trial court determined that "array" meant a collection of Flash EEPROM memory cells on one or more EEPROM chips. SanDisk argues, to the contrary, that by the plain meaning expressed in technical dictionaries "array" refers only to a collection of cells on a single integrated circuit or chip. Ritek argues that the '987 patent uses array in a specific sense, at odds with the plain meaning, but consistent with the trial court's interpretation. Ritek further argues that judicial estoppel applies, with special force, to the proper reading of "array."

As noted above, the difference does not alter the trial court's judgment of no infringement. The judgment does not depend on the choice between these disputed meanings of "array". It turns, instead, on the district court's reading of the partitioning requirements in the claims. Because this court re-

views judgments rather than claim construction orders, we find it unnecessary at this point to decide this dispute.

III.

[5] Pretec urges the court to affirm the judgment of no infringement in view of its arguments concerning the meaning of "corresponds" in claims 1 and 10. Pretec made the same claim construction and infringement arguments to the trial court after the relevant cut-off dates under the Northern District's Patent Local Rules and the trial court's scheduling order. The district court refused to entertain Pretec's untimely arguments. As explained in *Genentech, Inc. v. Amgen, Inc.*, 289 F.3d 761, 774 [62 USPQ2d 1640] (Fed. Cir. 2002), this court gives broad deference to the trial court's application of local procedural rules in view of the trial court's need to control the parties and flow of litigation before it. "[T]his court defers to the district court when interpreting and enforcing local rules so as not to frustrate local attempts to manage patent cases according to prescribed guidelines." *Id.* The district court's application of the local rules are within its sound discretion, and when reviewing that exercise of discretion, "this court determines whether (1) the decision was clearly unreasonable, arbitrary, or fanciful; (2) the decision was based on an erroneous conclusion of law; (3) the court's findings were clearly erroneous; or (4) the record contains no evidence upon which the court rationally could have based its decision." *Id.* None of these criteria for setting aside the district court's ruling are satisfied here. In sum, Pretec shows no abuse of discretion in the district court's ruling, and indeed we discern none.⁴

IV.

The district court erred in its claim construction. The limiting preambles in claims 1 and 10 are written in open language, and the claims are not limited to memory systems in which every memory cell is grouped into a partitioned sector. The judgment of no infringement rests on an erroneous claim construction, and the court vacates it. The case is remanded for further proceedings.

⁴ We do not decide whether, at trial on the merits, Pretec can or should be precluded from presenting these claim construction and non-infringement arguments.

VACATED AND REMANDED

Each side shall bear its own costs.

Benson v. Ginter

**U.S. Patent and Trademark Office
Board of Patent Appeals and Interferences**

Interference No. 105,142

Decided November 17, 2004

(Nonprecedential)

PATENTS

- [1] Practice and procedure in Patent and Trademark Office — Prosecution — Duty of candor — Materiality (§ 110.0903.04)

Practice and procedure in Patent and Trademark Office — Interference — Burden of proof (§ 110.1707)

Practice and procedure in Patent and Trademark Office — Interference — Motions (§ 110.1717)

Party filing preliminary motion in interference has burden of establishing that it is entitled to relief requested, which, for motion alleging inequitable conduct due to failure to disclose material information, requires at least threshold level of materiality of undisclosed reference, and threshold level of intent to mislead or deceive U.S. Patent and Trademark Office; in present case, senior party's motion alleging that junior party violated duty of disclosure must be dismissed without consideration of junior party's opposition or senior party's reply, since senior party's exhibit purporting to illustrate allegation of inequitable conduct merely shows drawing of invention described in interference counts, and does not indicate closest known prior art, since senior party has not established that text document to which senior party refers in its allegations was written by individual subject to duty of disclosure, and since, even if author of document was under such duty, senior party's motion paper does not give rise to inference of threshold level of intent to mislead or deceive PTO, and senior party's counsel declined prior opportunity to request taking of testimony in support of its motion.

- [2] Practice and procedure in Patent and Trademark Office — Prosecution —

Filing date (§ 110.0906)

Practice and procedure in Patent and Trademark Office — Interference — Motions (§ 110.1717)

Preliminary motion of junior party in interference seeking to be accorded benefit of filing date of foreign application is granted, since senior party did not file opposition, and since motion sets forth prima facie case of entitlement to relief requested.

- [3] Practice and procedure in Patent and Trademark Office — Interference — Counts (§ 110.1703)

Practice and procedure in Patent and Trademark Office — Interference — Motions (§ 110.1717)

Preliminary motion of junior party in interference seeking to redefine interference by substituting proposed count for existing count is granted, even though junior party perfected its claim of priority to foreign application in order to overcome rejection of claims including those corresponding to existing count, since reasonable conclusion is that examiner recommending interference was asserting that claims were allowable after junior party overcame rejection, since patentability of subject matter of proposed new count is not at issue, since testimony of junior party's expert, who concluded that relevant language in existing count is essentially same as corresponding portion of proposed count, will be accorded some weight in that language in counts is similar and expert is entitled to give opinion based on prior professional and technical experience, and since scope of proposed count, as whole, is clearly different from that of existing count, and junior party does not suggest otherwise.

- [4] Practice and procedure in Patent and Trademark Office — Prosecution — Disclaimer (§ 110.0925)

Practice and procedure in Patent and Trademark Office — Interference — Motions (§ 110.1717)

Preliminary motions of junior party in interference, alleging that senior party's involved claims are unpatentable for obviousness-type double patenting, are considered withdrawn, since senior party filed terminal disclaimers to obviate charges of double patenting.

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of

**CERTAIN NOR AND NAND FLASH MEMORY
DEVICES AND PRODUCTS CONTAINING SAME**

Inv. No. 337-TA-560

**INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND
RECOMMENDED DETERMINATION ON REMEDY AND BOND**

Administrative Law Judge Charles E. Bullock

(June 1, 2007)

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TABLE OF CONTENTS

LIST OF ABBREVIATIONS	viii
DISCUSSION	3
I. Introduction	3
A. Procedural History	3
1. Prior Investigations	3
a. Inv. No. 337-TA-382	3
b. Inv. No. 337-TA-526	3
2. Current Investigation	4
B. The Parties	12
1. Complainant	12
2. Respondents	12
C. Overview of the Technology	12
D. The Patents at Issue	13
1. The '338 Patent	13
2. The '517 Patent	14
E. The Products at Issue	14
1. SanDisk's Products	14
2. ST's Products	15
II. Jurisdiction and Importation	16
A. Subject Matter Jurisdiction	16
B. Personal Jurisdiction	17

III.	Relevant Law	17
A.	Claim Construction	17
B.	Infringement	22
1.	Literal Infringement	22
2.	Indirect Infringement	23
C.	Domestic Industry	24
D.	Validity	26
1.	Anticipation, 35 U.S.C. §§ 102 (a), (b) and (e)	27
2.	Obviousness, 35 U.S.C. § 103 (a)	28
3.	Written Description/Enablement, 35 U.S.C. § 112, ¶ 1	31
E.	Enforceability	33
1.	Inequitable Conduct	33
2.	Improper Inventorship, 35 U.S.C. § 102(f)	35
IV.	The '338 Patent	37
V.	The '517 Patent	46
A.	Claim Construction	46
1.	Asserted Claims	46
2.	Disputed Claim Terms	47
a.	Claim 1 - In General	47
b.	"EEPROM system" (claim 1)	51
c.	"Electrically floating gate" (claim 1)	52
d.	"Alterable" (claim 1)	53

e.	“Appropriate voltage conditions” (claim 1)	54
f.	“Applying said appropriate voltage conditions in parallel to a plurality of said memory cells” (claims 1 and 7)	56
g.	“Determining the threshold level ranges in which individual ones of said plurality of memory cells lie” (claim 1)	58
h.	“Terminating said application of appropriate voltage conditions to individual ones of said plurality of memory cells” (claim 1)	62
i.	“Continuing to apply said appropriate voltage conditions to others of said plurality of cells” (claim 1)	65
j.	“Until all of the plurality of cells are determined to have reached their desired threshold level ranges” (claim 1)	67
k.	“Breakpoint threshold level” (claim 5)	70
l.	“Blocks” (claims 7 and 8)	70
m.	“A chunk of input data being programmed into the memory system” (claims 12 and 13)	73
n.	“Comparing the threshold levels of the plurality of cells with the chunk of input data” (claim 13)	74
o.	“Cache memory” (claim 14)	76
B.	Infringement	78
1.	Claim 1	79
a.	Preamble	79
b.	First Limitation	81
c.	Second Limitation	82
	(1) ST NAND	82
	(2) ST NOR	86
d.	Third Limitation	89

e.	Fourth Limitation	91
f.	Conclusion	92
2.	Claim 3	92
3.	Claim 5	93
4.	Claim 6	93
5.	Claim 7	95
6.	Claim 8	95
7.	Claim 10	96
8.	Claim 12	97
9.	Claim 13	99
10.	Claim 14	100
11.	Indirect Infringement	101
a.	Induced Infringement	101
b.	Contributory Infringement	105
C.	Domestic Industry	108
1.	Technical Prong	108
a.	Claim 1	109
b.	Dependent Claims	113
2.	Economic Prong	114
D.	Validity	114
1.	Ordinary Skill in the Art	114
2.	Anticipation	115

a.	GB '145	115
b.	The '179 Patent	117
c.	M293	120
3.	Obviousness	121
a.	JP100	123
b.	JP100 and the '179 Patent	127
c.	JP100 and the '344 patent	131
d.	JP100 and the '871 patent	134
e.	JP 100 and the '541 patent	136
f.	Secondary Considerations	137
4.	Lack of Enablement/Inadequate Written Description/Best Mode	141
E.	Unenforceability	141
	CONCLUSIONS OF LAW	142
	INITIAL DETERMINATION	144
	RECOMMENDED DETERMINATION ON REMEDY AND BOND	146
VI.	Remedy and Bonding	146
A.	Limited Exclusion Order	146
B.	Downstream Products	147
1.	Factor 1: The value of the infringing articles compared to the value of the downstream products in which they are incorporated	149
2.	Factor 2: The identity of the manufacturer of the downstream products (<i>i.e.</i> , are the downstream products manufactured by the party found to have committed the unfair act, or by third parties)	150

3.	Factor 3: The incremental value to the complainant for excluding the downstream products	151
4.	Factor 4: The incremental detriment to respondents if the products are excluded	152
5.	Factor 5: The burden borne by third parties as a result of excluding downstream products	154
6.	Factor 6: The availability of alternative downstream products that do not contain the infringing articles	154
7.	Factor 7: The likelihood that the downstream products actually contain the infringing article and, thus, are subject to the exclusion order	155
8.	Factor 8: The opportunity for evasion of an exclusion order	156
9.	Factor 9: The enforceability of an order by Customs	157
10.	Conclusion	158
C.	Cease and Desist Order	159
D.	Bond During Presidential Review Period	159
APPENDIX OF EXHIBIT LISTS		A1

LIST OF ABBREVIATIONS

CDX	Complainant's demonstrative exhibit
CFF	Complainant's proposed findings of fact
CIB	Complainant's initial post-hearing brief
CORFF	Complainant's objections to Respondents' proposed findings of fact
COSFF	Complainant's objections to Staff's proposed findings of fact
CPX	Complainant's physical exhibit
CRB	Complainant's reply post-hearing brief
CX	Complainant's exhibit
Dep	Deposition
JX	Joint Exhibit
RDX	Respondents' demonstrative exhibit
RFF	Respondents' proposed findings of fact
RIB	Respondents' initial post-hearing brief
ROCFF	Respondents' objections to Complainant's proposed findings of fact
ROSFF	Respondents' objections to Staff's proposed findings of fact
RPX	Respondents' physical exhibit
RRB	Respondents' reply post-hearing brief
RX	Respondents' exhibit
SFF	Staff's proposed findings of fact
SIB	Staff's initial post-hearing brief
SOCFF	Staff's objections to Complainant's proposed findings of fact
SORFF	Staff's objections to Respondents' proposed findings of fact
SRB	Staff's reply post-hearing brief
Tr.	Transcript

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of

**CERTAIN NOR AND NAND FLASH MEMORY
DEVICES AND PRODUCTS CONTAINING SAME**

Inv. No. 337-TA-560

**INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND
RECOMMENDED DETERMINATION ON REMEDY AND BOND**

Administrative Law Judge Charles E. Bullock

(June 1, 2007)

Pursuant to the Notice of Investigation¹ and Rule 210.42(a) of the Rules of Practice and Procedure of the United States International Trade Commission, this is the Administrative Law Judge's Initial Determination in the matter of Certain NOR and NAND flash memory devices and products containing same, Investigation No. 337-TA-560.

The Administrative Law Judge hereby determines that a violation of Section 337 of the Tariff Act of 1930, as amended, has not been found in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain NOR and NAND flash memory devices and products containing same, in connection with claims 1, 3, 5, 6, 7, 8, 10, 12, 13, and 14 of U.S. Patent No. 5,991,517 and has not been found in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain NOR and NAND flash memory devices and products containing same, in connection with claims 8, 9, 11,

¹ 70 Fed. Reg. 61,841 (October 26, 2005).

27, 28, 32, 50, 51, and 64 of U.S. Patent No. 5,172,338. Furthermore, the Administrative Law Judge hereby determines that a domestic industry in the United States exists that practices U.S. Patent No. 5,991,517 and does not exist that practices U.S. Patent No. 5,172,338.

DISCUSSION

I. Introduction

A. Procedural History

1. Prior Investigations

a. Inv. No. 337-TA-382

The '338 patent has been asserted in two prior Section 337 investigations. The first was Inv. No. 337-TA-382, *Certain Flash Memory Circuits and Products Containing Same* ("the 382 investigation" or "*Certain Flash Memory Circuits*"), which involved SanDisk and Respondents Samsung Electric Company, Ltd. and Samsung Semiconductor, Inc. (collectively "Samsung"), and was before ALJ Harris. In the '382 investigation, ALJ Harris found that Samsung infringed claim 27 of the '338 patent and that SanDisk met the technical prong of domestic industry. The Commission did not review ALJ Harris' determination on these issues. The case eventually settled.

b. Inv. No. 337-TA-526

The second investigation involving the '338 patent was Inv. No. 337-TA-526, *Certain NAND Flash Memory Circuits and Products Containing Same* ("the 526 investigation" or "*Certain NAND Flash Memory Circuits*"), which involved SanDisk and ST, and was before ALJ Luckern. In the '526 investigation, ALJ Luckern found that ST's NAND products did not infringe claims 27, 28, or 32 of the '338 patent and that SanDisk's NAND products did not meet the technical prong of domestic industry. The Commission affirmed ALJ Luckern's findings on these issues. The Federal Circuit affirmed the Commission's decision without a published opinion on March 6, 2007.²

² See *SanDisk Corp. v. Int'l Trade Comm'n*, Docket No. 06-1187 (Fed. Cir., Mar. 6, 2007) (affirmed per Rule 36 without published opinion) ("*SanDisk*").

2. Current Investigation

On January 10, 2006, Complainant SanDisk Corporation ("SanDisk") filed a complaint with the Commission pursuant to Section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337. The complaint was supplemented on January 24, 2006. The complaint, as supplemented, asserts unfair methods of competition and unfair acts in violation of Section 337 by Respondents STMicroelectronics N.V., and STMicroelectronics, Inc. ("collectively ST") in connection with the importation, sale for importation, and sale within the United States after importation of certain NOR and NAND flash memory devices and products containing same.

The complaint accuses ST's products of infringing various claims of the following three U.S. Patents owned by SanDisk: claims 27, 28, 32, 50, 51, and 64 of U.S. Patent No. 5,172,338 ("the '338 patent"); claims 1-8 and 10-14 of U.S. Patent No. 5,991,517 ("the '517 patent"); and claims 7 and 10 of U.S. Patent No. 6,542,956 ("the '956 patent"). The complaint further alleges that there exists a domestic industry with respect to the patents-at-issue. SanDisk seeks, among other things, a limited exclusion order of the infringing NOR and NAND flash memory devices and products containing same, including all downstream products containing the accused ST chips. On February 8, 2006, the Commission issued a notice of investigation that was subsequently published in the Federal Register on February 13, 2005.³ On February 14, 2006, the undersigned set a fourteen-month target date for the investigation, or April 13, 2007.⁴ ST filed a response to the complaint and notice of investigation on March 6, 2006, which was subsequently amended on June 5, 2006 and September 28, 2006.

³ See Notice of Investigation, 71 Fed. Reg. 7576 (February 13, 2006).

⁴ See Order No. 2 (February 14, 2006).

On April 13, 2006, SanDisk filed a motion for leave to amend the Complaint and Notice of Investigation, which was granted by initial determination in Order No. 4, issued on April 25, 2006. On May 17, 2006, the Commission issued a notice not to review the initial determination. Specifically, SanDisk moved to assert three additional claims from the '338 patent (claims 8, 9, and 11), one additional claim from the '956 patent (claim 11), and to accuse ST's NAND flash memory devices of infringing claims 3 and 5 of the '517 patent.

On March 31, 2006, ST filed a motion to terminate the investigation as to the '338 patent based on SanDisk having no domestic industry in the '338 patent, largely based on issue preclusion from the '526 investigation. On May 1, 2006, the undersigned denied the motion to terminate in Order No. 5. On May 8, 2006, ST filed a motion for leave to appeal Order No. 5, which was denied by Order No. 7, issued on May 22, 2006.

On May 17, 2006, SanDisk filed a motion for partial termination of the investigation with respect to the '956 patent, which was granted by initial determination in Order No. 8, issued on June 1, 2006. On June 19, 2006, the Commission issued a notice not to review the initial determination.

On May 15, 2006, the Commission Investigative Staff ("Staff") filed a motion to amend the notice of investigation, which was denied in Order No. 9, issued on June 1, 2006. Specifically, Staff moved to amend the notice of investigation to make the case caption (which read "Certain NOR and NAND Flash Memory Devices and Products Containing Same) consistent with the body of the notice, which failed to include the "products containing same" language. The undersigned ruled that, while it was understandable that the omission of the standard "products containing same" language may have been an inadvertent error, good cause did not exist to amend the notice of investigation at that time, which was more than four months after the notice of investigation had been issued,

because of the potential prejudice to the public interest (including non-parties to the investigation), and parties to the investigation.

On June 7, 2006, Staff filed a motion for reconsideration of Order No. 9, or in the alternative, for leave to seek interlocutory review, which was denied in Order No. 14, issued on July 6, 2006. On June 8, 2006, SanDisk filed a motion for reconsideration, or in the alternative, clarification of Order No. 9, which was granted in part by Order No. 14. On June 15, 2006, SanDisk filed a motion for leave to amend the complaint to remove any ambiguity regarding the scope of the remedy sought by SanDisk (which includes a remedy against third party downstream products that incorporate the infringing ST chips), which was denied by Order No. 14.

In Order No. 14, the undersigned clarified certain aspects of Order No. 9, including (1) that the language in the body of the notice of investigation defines the parameters of the scope of the investigation, not the case caption, and (2) that ST's downstream products are not within the scope of the investigation. In that order, the undersigned clarified that the purpose of the notice of investigation differs from the complaint. Specifically, the notice of investigation determines the scope of the investigation, while the complaint serves as a notice function, detailing the specific claims on which a complainant is relying. The undersigned noted that the Commission has the authority to institute an investigation that covers downstream products, regardless of whether a complainant requests such relief in the complaint. But, the complaint is what puts the other parties on notice that complainant intends to assert narrower relief. The undersigned determined that, in the case where the scope of the notice of investigation is narrower than the relief sought in the complaint, the notice of investigation must govern.

On July 24, 2006, the Commission, *sua sponte*, issued a "Notice of Correction" regarding

the notice of investigation, adding the "and products containing same" language to the body of the notice. The notice also stated that the Commission "expects that the administrative law judge will extend the target date for completion of the investigation to the extent necessary to avoid any prejudice to the parties." On August 15, 2006, the undersigned issued Order No. 18, an initial determination granting SanDisk's renewed second motion for leave to amend the complaint based on the Commission's notice of correction, and to extend the target date by four months. On September 26, 2006, the Commission issued a notice not to review the initial determination.

On July 27, 2006, SanDisk filed a motion to request judicial enforcement of subpoena to Intel Corporation ("Intel"). According to SanDisk, it served a subpoena on Intel requesting discovery on the design and operation of Intel's licensed flash memory products and on Intel's related expenditures in the United States, which was essential to SanDisk's claim of a domestic industry in the '338 patent because SanDisk's claim of domestic industry relies solely on Intel's practice of the '338 patent and that the information could only be obtained from Intel. On August 15, 2006, the undersigned issued Order No. 21, which denied the motion. The undersigned ruled that

This is not the usual type of request for judicial enforcement of a subpoena because it involves information essential to proving Complainant's own domestic industry based on a licensing agreement with a third-party for a patent that has already been adjudicated at the Commission. While the undersigned finds that Complainant otherwise could have made a proper showing of purpose, relevance and reasonableness, that there are other considerations that warrant against certifying the judicial enforcement request to the Commission.

First, the undersigned does not find that this is a situation where a third-party receives a subpoena and simply ignores it, believing that the Commission's subpoenas are rarely enforced so that there is little incentive for them to produce relevant information in response to a Commission subpoena. Based on the pleadings filed by Intel, Intel asserts that it has already turned over 7,000 pages of circuit schematic diagrams as well as several thousand more pages of design guides and internal architecture specifications detailing the structure and operation of Intel's products. The fact that such documents were produced in what SanDisk considers to

be an “inconvenient format and are difficult and time-consuming to analyze” should not be held against Intel. Perhaps if SanDisk would have requested such information from Intel before it filed the complaint, SanDisk would have had more time to analyze the documents without any time constraints and more fully evaluate whether Intel’s NOR flash memory products practice the ‘338 patent.

Second, the undersigned finds it troubling that Complainant did not have the requisite information needed to meet its burden of proof on domestic industry before filing the complaint or that it cannot obtain this information from Intel based on its already existing business/license relationship. This is somewhat surprising given Complainant’s history of already having adjudicated the ‘338 patent here at the Commission. The undersigned finds it disturbing that SanDisk did not even approach Intel prior to filing the complaint in an attempt to ascertain whether Intel’s NOR flash memory products practice the ‘338 patent, especially since it appears that SanDisk is relying on the doctrine of equivalents for certain claim limitations. Complainant had complete control of the timing of filing the complaint and it could have waited to file the complaint after it received information from Intel in order to have a good faith basis to assert a domestic industry in the ‘338 patent.⁵

On August 28, 2006, SanDisk filed a motion for reconsideration of Order No. 21 with respect to the economic prong of the domestic industry requirement. On September 15, 2006, the undersigned issued Order No. 26, denying the motion. The undersigned ruled that

In general, requests for reconsideration “must be confined to new questions raised by the contested determination or the action to be taken thereunder—*questions upon which the moving party had no previous opportunity to submit arguments.*” SanDisk had the opportunity to clearly raise the issue of economic prong documents in its original motion for judicial enforcement. While it is clear that the subpoena covers issues related to both the technical and economic prong of domestic industry, the moving papers focused exclusively on technical prong (with a few conclusory statements regarding economic prong), so the undersigned’s order naturally focused on technical prong as well, even though the order was not limited to technical prong and was written in terms of “domestic industry” in general. Accordingly, the undersigned finds that no new questions have been raised since the undersigned’s ruling in Order No. 21 because SanDisk had the opportunity to present its arguments regarding economic prong documents at the time of its original motion for judicial enforcement, and that because it did not do so, no new questions have been raised.

Furthermore, the undersigned recognizes that there is no requirement under

⁵ See Order No. 21 (August 15, 2006) (footnotes omitted).

Section 337 that a patent holder, who is relying on domestic industry based on the operations of a licensee, must consult with and obtain the cooperation of that licensee before requesting institution of a Section 337 investigation. The undersigned did not base his ruling in Order No. 21 solely because SanDisk did not consult with Intel before filing the complaint. Rather, all the facts and circumstances were considered and the fact that SanDisk did not consult with Intel before the complaint was filed was merely one of the factors that the undersigned considered, which weighed against judicial enforcement. The undersigned's intention in noting that SanDisk's failure to consult with Intel as a factor against judicial enforcement was that SanDisk, as the complainant in this investigation who had already litigated the '338 patent at the Commission twice before, was that a complainant who has the burden of proof with regards to domestic industry should have a good faith basis for establishing that such industry exists before the complaint is filed and that informing a licensee before a case is filed could be beneficial.⁶

On September 12, 2006, SanDisk filed a motion for partial termination of the investigation with respect to claims 1, 2, and 4 of the '517 patent. On October 10, 2006, the undersigned filed Order No. 30, an initial determination granting the motion in part. The undersigned granted the motion with respect to claims 2 and 4, but denied the motion with respect to claim 1. On October 27, 2006, the Commission issued a notice not to review the initial determination.

On September 25, 2006, SanDisk filed a motion for summary determination on the economic prong of the domestic industry requirement in the '517 patent. On November 17, 2006, the undersigned issued Order No. 37, an initial determination granting the motion. On December 8, 2006, the Commission issued a notice not to review the initial determination.

On September 25, 2006, ST filed a motion for summary determination of non-infringement with respect to ST's SLC NOR, 1G F70 NAND, [] and [] products. On November 17, 2006, the undersigned issued Order No. 38, an initial determination granting in part ST's motion. Specifically, the undersigned determined that there was no infringement with

⁶ See Order No. 26 (September 15, 2006) (footnotes omitted).

respect to ST's SLC NOR products. As to ST's 1G F70 NAND,[] and [] products, the undersigned made no determination regarding infringement, but terminated those products from the investigation and ruled that those products would not be covered by an exclusion order, if applicable.

The parties have stipulated as to certain material facts.⁷ Particular stipulated facts that are relevant to this Initial Determination are cited accordingly.

An evidentiary hearing on liability was conducted before the undersigned from December 4-15, 2006. In support of its case-in-chief and rebuttal case, SanDisk called the following witnesses:

- Mr. Eli Harari (chairman and CEO of SanDisk);⁸
- Sanjay Mehrotra (president of SanDisk);⁹
- Dr. Khandker Quader (VP for memory design at SanDisk);¹⁰
- Gerald Parsons, Esq. (SanDisk's patent prosecution attorney);¹¹
- Brian Napper (SanDisk's domestic industry expert);¹²
- Sakhawat Khan (SanDisk's expert);¹³
- V. Thomas Rhyne (SanDisk's expert);¹⁴ and
- Dr. G. R. Mohan Rao (SanDisk's expert).¹⁵

⁷ See JX-138, JX-139C, and JX-148.

⁸ CX-2225C (Harari Direct); CX-2294C (Harari Rebuttal).

⁹ CX-2226C (Mehrotra Direct); CX-2295C (Mehrotra Rebuttal).

¹⁰ CX-2227C (Quader Direct).

¹¹ CX-2232C (Parsons Direct).

¹² CX-2234C (Napper Direct); CX-2296C (Napper Rebuttal).

¹³ CX-2230C (Khan Direct).

¹⁴ CX-2229C (Rhyne Direct); CX-2324C (Rhyne Supplemental Direct); CX-2298C (Rhyne Rebuttal).

¹⁵ CX-2235C (Rao Direct).

In support of its case-in-chief and rebuttal case, ST called the following witnesses:

- Dr. Vivek Subramanian (ST's expert);¹⁶
- Giulio Casagrande (ST's group VP & director of R&D in the memory products group);¹⁷
- Corrado Villa (ST design director of the wireless flash division of the memory products group);¹⁸
- Mauro Sali (ST product design director);¹⁹
- Richard Pashley (ST's claim construction expert);²⁰
- Carla Mulhern (ST's remedy and bonding expert);²¹ and
- Martin Adelman (ST's patent procedures expert).²²

In addition, various deposition testimony was received into evidence in lieu of direct witness statements or live testimony.

After the hearing, post-hearing briefs and reply briefs, together with proposed findings of fact, conclusions of law and rebuttals to the same, were filed on January 8, 2007 and January 19, 2007, respectively.

On January 16, 2007, the undersigned issued Order No. 43, an initial determination extending the target date of the investigation by one and a half months, to October 1, 2007. The Commission did not review this Initial Determination.

¹⁶ RX-1801C (Subramanian Direct); RX-2153C (Subramanian Rebuttal).

¹⁷ RX-1804C (Casagrande Direct).

¹⁸ RX-2155C (Villa Rebuttal).

¹⁹ RX-2156C (Sali Rebuttal).

²⁰ RX-1802C (Pashley Direct).

²¹ RX-1800C (Mulhern Direct); RX-2154C (Mulhern Rebuttal).

²² RX-1803C (Adelman Direct).

B. The Parties

1. Complainant

Complainant SanDisk Corporation ("SanDisk") is a Delaware corporation with its headquarters in Milpitas, California. Prior to 1995, SanDisk was known as "SunDisk Corporation."

2. Respondents

Respondent STMicroelectronics N.V. is a Netherlands corporation with its principal place of business in Geneva, Switzerland. Respondent STMicroelectronics, Inc. is a Delaware corporation with its principal place of business in Carrollton, Texas. Prior to 1998, ST was known as SGS-Thompson Microelectronics.

C. Overview of the Technology

At issue in this investigation are certain NOR and NAND flash memory devices and products containing same. Both the '517 and '338 patents relate to improving the performance and accuracy of flash memory devices and systems. "EEPROM" stands for "electrically erasable programmable read-only memory," which is a type of non-volatile memory chip(s). Non-volatile memory chips include memory cells that contain a structure (*e.g.*, a floating gate) that retains its data content even when power is removed from the memory chip. Memory that retains information when power is removed is useful in many applications, including computer systems.

An EEPROM includes a source, a drain, a gate (called a "control" gate), a floating gate, and a substrate. If the memory cell stores more than one bit of information ("11", "10", "01" or "00"), the EEPROM is called a multi-level cell (MLC) device. The basic unit of memory in a flash EEPROM device is referred as a "cell." Memory cells are based on a type of transistor – the metal oxide semiconductor field effect transistor ("MOSFET"). EEPROM cells consist of a MOSFET

with an additional "floating" gate between the control gate and the substrate for storing one or more bits of information. One method of placing electrons on a floating gate is called Hot Electron Injection ("HEI"). A cell undergoing HEI has its source grounded to 0 volts and the voltage at its drain terminal and its control gate raised to a high voltage. Another method for placing electrons on a floating gate is Fowler-Nordheim Tunneling.

In flash EEPROM devices, memory cells are arranged into rows, connected with wordlines and columns, connected via bit lines, which together form an array. Two of the most common EEPROM array architectures are NAND and NOR architectures. In a NAND EEPROM array, all cells in a column are linked together in what is referred to as a "NAND string." In a NAND string, access to a given cell in a column goes through the other cells in the NAND string. In a NOR architecture, each memory cell is at the intersection of a wordline and a bitline.

D. The Patents at Issue

1. The '338 Patent

The '338 patent is entitled "Multi-state EEPROM read and write circuits and techniques" which was issued on December 15, 1992, based on Application Serial No. 508,273, filed on April 11, 1990. The named inventors are Sanjah Mehrotra and Eliyahou Harari,²³ and the patent was assigned to the SunDisk Corporation. SanDisk is the current owner of the '338 patent by assignment. On July 8, 1997, a reexamination certificate was issued, along with a certificate of correction. The '338 patent has a total of 65 claims.²⁴ Three independent claims, claims 8, 27, and

²³ Note that Winston Lee is noted as an inventor, but a Certificate of Correction, issued on November 2, 1993, deleted him as a named inventor.

²⁴ The '338 patent was reexamined, where it was determined that the patentability of claims 1-31, 35-43, and 45-47 is confirmed, claims 32 and 44 were determined to be patentable as amended, (continued...)

32 are at issue here. Dependent claims 9, 11, 28, 50, 51, and 64 are also at issue here.²⁵

2. The '517 Patent

The '517 patent is entitled "Flash EEPROM system with cell by cell programming verification" which was issued on November 23, 1999, based on Application Serial No. 08/771,708, filed on December 20, 1996. The named inventors are Eliyahou Harari, Robert D. Norman, and Sanjay Mehrotra, and the patent was assigned to SanDisk Corporation, the current owner of the '517 patent. The '517 patent has a total of 39 claims. One independent claim, claim 1 is at issue here. Dependent claims 3, 5-8, and 10-14 are also at issue here.²⁶

E. The Products at Issue

1. SanDisk's Products

SanDisk is in the semiconductor and consumer electronics business. SanDisk produces NAND flash components, as well as controllers, and packages them into products such as flash memory cards, MP3 players, and USB flash drives. SanDisk asserts that its [] flash memory satisfies the technical prong of the domestic industry requirement for the '517 patent.

²⁴(...continued)

claims 33 and 34, dependent on an amended claim, were determined to be patentable, while claims 48-65 were added and determined to be patentable.

²⁵ See CX-98/RX-1 ("the '338 patent"); CX-100/RX-3 ("the '338 prosecution history"); CX-102/RX-5 ("the '338 reexamination").

The undersigned notes that the Ground Rules specifically provide that parties are supposed to exchange exhibit lists with each other prior to date exhibits are to be exchanged to eliminate any duplicate exhibits or renumber the exhibits as joint exhibits. See Ground Rule 9.4.1. The undersigned can find no reason why the parties should not be able to agree to have the patents at issue, along with their corresponding prosecution histories, to be labeled as joint exhibits. Because the parties failed to adhere to this Ground Rule, it makes referencing specific pages in the prosecution history quite burdensome because the parties have put different bates numbers on their own exhibits when referring to the same document. The undersigned has attempted to cross-reference such bates numbers in as many places as possible.

²⁶ See CX-99/RX-2 ("the '517 patent"); CX-103/RX-4 ("the '517 prosecution history").

The parties have agreed that SanDisk's [] is representative of the design of SanDisk's other NAND flash memories including the following chips: []

] ²⁷

SanDisk relies on the following Intel MLC NOR products for domestic industry in the '338 patent: L18/L30 StrataFlash, code named [], K3/K18 StrataFlash, code named [] and J3 StrataFlash, code named []

2. ST's Products

ST produces chips and flash cards, and also sells its products for use in mobile phones, automotive, disc drive, computer, and consumer electronics applications. SanDisk accuses ST's [] MLC NOR chips of infringing claims 8, 9, 27, 28, 32, 50, and 64 of the '338 patent, and claims 1, 3, 5-8, 10, 12-14 of the '517 patent. In addition SanDisk accuses ST's SLC NAND chips, as well as certain versions of the 4G F90 MLC NAND chip, to infringe claims 1, 3, 5-8, 10, and 12 of the '517 patent. The parties have agreed that the design of the [] is representative of the [] and that the operation of the [] is representative of the design of the W8EL.²⁸ Specifically, SanDisk accuses the following ST products as infringing the asserted patents:

- [] MLC NOR flash memory chips: M30L0T7000, M36LLT7760, M25P128, M58LT128G, M58LT256G, M36L0T7040, M36L0R7060, M30L0T8000, M30L0T8800, M30L0T8860, M30L0T8888, M36L0T8060, M36L0R8860, M36LLR8870, M39L0R8070, M36LNR8860, M36L0R8050, M36L0R8060, M36L0T8050, M36L0T7060, M30L0R7000, M58LR128G, M58WR128FU, M36L0R7040, M36L0R7050, M30L0R8000, M58LR256GU, M30L0R8800,

²⁷ JX-139C (Stipulation Regarding Representative Products) at 3.

²⁸ JX-139C (Stipulation) at ¶¶ 2-4.

M39LLR8870, M36LLR8860, M39LOR8870, M36LOR8870, M36LLR8760, M36LOR8070, M39POR8070, M39POR8060, M36LOR8060, M36POR8060;

• [] MLC NOR flash memory chips: M39POR9970, M39LOR9070, M39POR9070, M36POR9070, M39POR9080, M36POR9080, M36POR9060; and

• NAND flash memory chips: 512 Mb F12 NAND, 256 Mb F12 NAND, 128 Mb F90 NAND, 256 Mb F90 NAND, 512 Mb F90 NAND (Small Page), 512 Mb F90 NAND (Large Page), 1 Gb F90 NAND, 2 Gb F90 NAND, 4 Gb F90 MLC NAND, 2 Gb F70 NAND, and 4 Gb F70 NAND.

II. Jurisdiction and Importation

Section 337 confers subject matter jurisdiction on the International Trade Commission to investigate, and if appropriate, to provide a remedy for, unfair acts and unfair methods of competition in the importation of articles into the United States. In order to have the power to decide a case, a court or agency must have both subject matter jurisdiction, and jurisdiction over either the parties or the property involved.²⁹

A. Subject Matter Jurisdiction

The complaint alleges that ST has violated Subsection 337(a)(1)(A) and (B) in the importation and sale of products that infringe the asserted patents. ST has admitted that it has imported millions of dollars of accused products into the United States and that it has [

] accused chips in inventory in the United States.³⁰ Accordingly, the Commission has subject matter jurisdiction over ST in this investigation.³¹

²⁹ 19 U.S.C. § 1337; also see *Certain Steel Rod Treating Apparatus and Components Thereof*, Inv. No. 337-TA-97, Commission Memorandum Opinion, 215 U.S.P.Q. 229, 231 (1981) ("*Certain Steel Rod*").

³⁰ ST's Response to Second Amended Complaint at 1; JX-135C (ST's Interrogatory Responses) at 9-11; CX-1871C (Americas Inventory); CX-2234C (Napper Direct) at 67-68.

³¹ See *Amgen, Inc. v. U.S. Int'l Trade Comm'n*, 902 F.2d 1532, 1536 (Fed. Cir. 1990) ("*Amgen*").

B. Personal Jurisdiction

ST has responded to the complaint and notice of investigation, participated in the investigation, including participating in discovery, made an appearance at the hearing, and submitted post-hearing briefs, thereby submitting to the personal jurisdiction of the Commission.³²

III. Relevant Law

A. Claim Construction

Analyzing whether a patent is infringed “entails two steps. The first step is determining the meaning and scope of the patent claims asserted to be infringed. The second step is comparing the properly construed claims to the device or process accused of infringing.”³³ The first step is a question of law, whereas the second step is a factual determination.³⁴ Concerning the first step of claim construction, “[i]t is well-settled that, in interpreting an asserted claim, the court should look first to the intrinsic evidence of record, *i.e.*, the patent itself, including the claims, the specification and, if in evidence, the prosecution history Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language.”³⁵

“In construing claims, the analytical focus must begin and remain centered on the language of the claims themselves, for it is that language that the patentee chose to use to ‘particularly point

³² See *Certain Miniature Hacksaws*, Inv. No. 337-TA-237, U.S.I.T.C. Pub. No. 1948, Initial Determination (unreviewed by Commission in relevant part) at 4, 1986 WL 379287 (U.S.I.T.C., October 15, 1986) (“*Certain Miniature Hacksaws*”).

³³ *Dow Chem. Co. v. United States*, 226 F.3d 1334, 1338 (Fed. Cir. 2000) (“*Dow Chemical*”), citing *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (*en banc*), *aff’d*, 517 U.S. 370 (1996) (“*Markman*”).

³⁴ *Markman*, *supra*.

³⁵ *Bell Atlantic Network Serv., Inc. v. Covad Communications Group, Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001) (“*Bell Atlantic*”). See also *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-17 (Fed. Cir. 2005) (“*Phillips*”), *cert. denied*, 126 S.Ct. 1332.

[] out and distinctly claim [] the subject matter which the patentee regards as his invention.”³⁶

“Quite apart from the written description and the prosecution history, the claims themselves provide substantial guidance as to the meaning of particular claim terms.”³⁷ Usage of a term in both the asserted and unasserted claims is “highly instructive” in determining the meaning of the same term in other claims.³⁸ “Furthermore, a claim term should be construed consistently with its appearance in other places in the same claim or in other claims of the same patent.”³⁹

“While not an absolute rule, all claim terms are presumed to have meaning in a claim.”⁴⁰ If the claim language is not clear on its face, “[t]hen we look to the rest of the intrinsic evidence, beginning with the specification and concluding with the prosecution history, if in evidence” for the purpose of “resolving, if possible, the lack of clarity.”⁴¹

There is a “heavy presumption” that claim terms are to be given “their ordinary and accustomed meaning as understood by one of ordinary skill in the art,” and in aid of this interpretation, “[d]ictionaries and technical treatises, which are extrinsic evidence, hold a ‘special place’ and may sometimes be considered along with the intrinsic evidence when determining the ordinary meaning of claim terms.”⁴² Caution must be used, however, when referring to non-

³⁶ *Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001) (“*Interactive Gift Express*”), citing 35 U.S.C. § 112, ¶ 2.

³⁷ *Phillips*, 415 F.3d at 1314 citing *Vitronics Corp. v. Conceptronic Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 2003) (“*Vitronics*”).

³⁸ *Id.*

³⁹ *Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1342 (Fed. Cir. 2001) (“*Rexnord*”) citing *Phonometrics Inc. v. Northern Telecom Inc.*, 133 F.3d 1459, 1465 (Fed. Cir. 1998) (“*Phonometrics*”).

⁴⁰ *Innova/Pure Water, Inc. v. Safari Water Filtration Sys.*, 381 F.3d 1111, 1119 (Fed. Cir. 2004) (“*Innova*”).

⁴¹ *Id.*

⁴² *Bell Atlantic*, 262 F.3d at 1267-68.

scientific dictionaries “lest dictionary definitions . . . be converted into technical terms of art having legal, not linguistic significance.”⁴³

The presumption in favor of according a claim term its ordinary meaning is overcome “(1) where the patentee has chosen to be his own lexicographer, or (2) where a claim term deprives the claim of clarity such that there is ‘no means by which the scope of the claim may be ascertained from the language used.’”⁴⁴ In this regard, “[t]he specification acts as a dictionary ‘when it expressly defines terms used in the claims or when it defines terms by implication.’”⁴⁵

The specification is considered “always highly relevant” to claim construction and “[u]sually, it is dispositive; it is the single best guide to the meaning of a disputed term.”⁴⁶ The prosecution history is also examined for a claim’s scope and meaning “to determine whether the patentee has relinquished a potential claim construction in an amendment to the claim or in an argument to overcome or distinguish a reference.”⁴⁷

“[I]f the meaning of the claim limitation is apparent from the intrinsic evidence alone, it is improper to rely on extrinsic evidence other than that used to ascertain the ordinary meaning of the claim limitation. [citation omitted] However, in the rare circumstance that the court is unable to determine the meaning of the asserted claims after assessing the intrinsic evidence, it may look to additional evidence that is extrinsic to the complete document record to help resolve any lack of clarity.”⁴⁸

⁴³ *Id.* at 1267 (internal quotation marks omitted).

⁴⁴ *Id.* at 1268.

⁴⁵ *Id.* See also *Phillips*, 415 F.3d at 1316.

⁴⁶ *Id.*

⁴⁷ *Id.*

⁴⁸ *Id.* at 1268-69.

“Extrinsic evidence consists of all evidence external to the patent and prosecution history”⁴⁹ It includes “such evidence as expert testimony, articles, and inventor testimony.”⁵⁰ But, “[i]f the intrinsic evidence resolves any ambiguity in a disputed claim, extrinsic evidence cannot be used to contradict the established meaning of the claim language.”⁵¹ “What is disapproved of is an attempt to use extrinsic evidence to arrive at a claim construction that is clearly at odds with the claim construction mandated by the claims themselves, the written description, and the prosecution history, in other words, with the written record of the patent.”⁵²

In interpreting particular limitations within each claim, “adding limitations to claims not required by the claim terms themselves, or unambiguously required by the specification or prosecution history, is impermissible.”⁵³ Usually, a patent is not limited to its preferred embodiments in the face of evidence of broader coverage by the claims.⁵⁴ A claim construction that excludes the preferred embodiment in the specification of a patent, however, is “rarely, if ever, correct.”⁵⁵

On the other hand, “there is sometimes ‘a fine line between reading a claim in light of the

⁴⁹ *Markman*, 52 F.3d at 980.

⁵⁰ *Bell Atlantic*, 262 F.3d at 1269.

⁵¹ *DeMarini Sports, Inc. v. Worth, Inc.*, 239 F.3d 1314, 1322-23 (Fed. Cir. 2001) (“*DeMarini*”).

⁵² *Markman*, 52 F.3d at 979.

⁵³ *Dayco Prod., Inc. v. Total Containment, Inc.*, 258 F.3d 1317, 1327 (Fed. Cir. 2001) (“*Dayco Products*”), citing *Laitram Corp. v. NEC Corp.*, 163 F.3d 1342, 1347 (Fed. Cir. 1998) (“*Laitram*”) (“a court may not import limitations from the written description into the claims”).

⁵⁴ *Acromed Corp. v. Sofamor Danek Group, Inc.*, 253 F.3d 1371, 1382-83 (Fed. Cir. 2001) (“*Acromed*”); *Electro Med. Sys. S.A. v. Cooper Life Sci., Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994) (“*Electro Med*”) (“particular embodiments appearing in a specification will not be read into the claims when the claim language is broader than such embodiments”).

⁵⁵ *Vitronics*, 90 F.3d at 1583-34.

specification, and reading a limitation into the claim from the specification.”⁵⁶ In order to negotiate this “fine line,” one guideline is that features of embodiments in the specification do not restrict patent claims “unless the patentee has demonstrated a clear intention to limit the claim scope using ‘words or expressions of manifest exclusion or restriction.’”⁵⁷ Another guideline is that features of an embodiment in the specification do not restrict claims unless the specification defines the claim terms “by implication” as may be “found in or ascertained by a reading of the patent documents.”⁵⁸ For the specification to limit the claims, there must be “a clear case of the disclaimer of subject matter that, absent the disclaimer, could have been considered to fall within the scope of the claim language.”⁵⁹

Claims amenable to more than one construction should, when it is reasonably possible to do so, be construed to preserve their validity.⁶⁰ A claim cannot, however, be construed contrary to its plain language.⁶¹ Claims cannot be judicially rewritten in order to fulfill the axiom of preserving

⁵⁶ *Bell Atlantic*, 262 F.3d at 1270.

⁵⁷ *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (“*Liebel-Flarsheim I*”).

⁵⁸ *Irdeto Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295, 1300 (Fed. Cir. 2004) (“*Irdeto*”).

⁵⁹ *Liebel-Flarsheim I*, 358 F.3d at 907. The Federal Circuit “has expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment.” *Liebel-Flarsheim I*, *supra*, 358 F.3d at 906 (emphasis added); also see, e.g., *Golight, Inc. v. Wal-Mart Stores, Inc.*, 355 F.3d 1327, 1331 (Fed. Cir. 2004) (“*Golight*”); *Bio-Technology General Corp. v. Duramed Pharmaceuticals, Inc.*, 325 F.3d 1356, 1362 (Fed. Cir. 2003) (“*Bio-Technology*”) (aspects of only embodiment described in specification not read into claims). The *Liebel-Flarsheim I* panel further held that even where a patent describes only a single embodiment, claims will not be “read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using ‘words or expressions of manifest exclusion or restriction.’” *Id.*

⁶⁰ *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1384 (Fed. Cir. 2001) (“*Karsten*”).

⁶¹ See *Rhine v. Casio, Inc.*, 183 F.3d 1342, 1345 (Fed. Cir. 1999) (“*Rhine*”).

their validity; “if the only claim construction that is consistent with the claim’s language and the written description renders the claim invalid, then the axiom does not apply and the claim is simply invalid.”⁶²

Pursuant to 35 U.S.C. § 112, ¶ 6, “[a]n element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.” An applicant may therefore “claim an element of a combination functionally, without reciting structures for performing those functions.”⁶³ To invoke this rule, “a claim limitation that actually uses the word ‘means’ will invoke a rebuttable presumption that § 112 ¶ 6 applies. By contrast, a claim term that does not use ‘means’ will trigger the rebuttable presumption that § 112 ¶ 6 does not apply.”⁶⁴ In general, the words “circuit” and “circuitry” connote sufficient structure in and of themselves so as not to be deemed as “means-plus-function” elements.⁶⁵

B. Infringement

1. Literal Infringement

Literal infringement is a question of fact.⁶⁶ Literal infringement requires the patentee to prove that the accused device contains each limitation of the asserted claim(s). Each element of a

⁶² *Id.*

⁶³ *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1371 (Fed. Cir.), *cert. denied*, 540 U.S. 1073 (2003) (“*Apex*”).

⁶⁴ *Linear Technology Corp. v. Impala Linear Corp.*, 379 F.3d 1311, 1319 (Fed. Cir. 2004) (“*Linear*”).

⁶⁵ See *Linear*, *supra*; *Apex*, 325 F.3d at 1374.

⁶⁶ *Tegal Corp. v. Tokyo Electron Am., Inc.*, 257 F.3d 1331, 1350 (Fed. Cir. 2001) (“*Tegal*”), *cert. denied*, 535 U.S. 927 (2002).

claim is considered material and essential, and in order to show literal infringement, every element must be found to be present in the accused device.⁶⁷ If any claim limitation is absent from the accused device, there is no literal infringement of that claim as a matter of law.⁶⁸

2. Indirect Infringement

To establish a claim for induced infringement, a complainant must show that a respondent has actively induced a person to make, use, or sell a product or use a method that falls within the scope of the claims of the patent at issue.⁶⁹ The required elements of a claim of induced infringement are: “(1) an act of direct infringement; (2) the accused infringer actively induced a third party to infringe the patent; and (3) the accused infringer knew or should have known that his actions would induce infringement.”⁷⁰

Under 35 U.S.C. § 271(c), a seller of a component of an infringing product can be held liable for contributory infringement if: “(1) there has been an act of direct infringement by a third party; (2) the accused contributory infringer knows that the combination for which its component was made was both patented and infringing; and (3) there are no substantial non-infringing uses for the component part, *i.e.*, the component is not a ‘staple article’ of commerce.”⁷¹

⁶⁷ *London v. Carson Pirie Scott & Co.*, 946 F.2d 1534, 1538 (Fed. Cir. 1991) (“*London*”).

⁶⁸ *Bayer AG v. Elan Pharm. Research Corp.*, 212 F.3d 1241, 1247 (Fed. Cir. 2000) (“*Bayer*”).

⁶⁹ 35 U.S.C. § 271(b).

⁷⁰ *Certain Flash Memory Circuits*, Inv. No. 337-TA-382, U.S.I.T.C. Pub. 3046, Commission Opinion on the Issues Under Review and on Remedy, the Public Interest, and Bonding, at 16, 1997 WL 817778 (U.S.I.T.C., July 1997) citing *Manville Sales Corp. v. Paramount Sys. Inc.*, 917 F.2d 544, 553 (Fed. Cir. 1990) (“*Manville*”). See also *Certain Headboxes and Papermaking Machine Forming Sections for the Continuous Production of Paper, and Components Thereof*, Inv. No. 337-TA-82, USITC Pub. No. 1138 at 18- 19 (1981) (“*Certain Headboxes*”).

⁷¹ *Certain Flash Memory*, Commission Opinion at 9-10.

C. Domestic Industry

In a patent-based complaint, a violation of Section 337 can be found “only if an industry in the United States, relating to the articles protected by the patent . . . concerned, exists or is in the process of being established.”⁷² This “domestic industry requirement” has an “economic” prong and a “technical” prong.

The term “domestic industry” in Section 337 is not defined by the statute, but the Commission has interpreted the intent of Section 337 to be “the protection of domestic manufacture of goods.”⁷³ The Commission has further stated that “[t]he scope of the domestic industry in patent-based investigations has been determined on a case by case basis in light of the realities of the marketplace and encompasses not only the manufacturing operations but may include, in addition, distribution, research and development and sales.”⁷⁴

In making this determination, Section 337(a)(2) provides that for investigations based on patent infringement, a violation can be found “only if an industry in the United States, relating to the articles protected by the patent . . . concerned, exists or is in the process of being established.” 19 U.S.C. § 1337(a)(2). Section 337(a)(3) sets forth the following economic criteria for determining the existence of a domestic industry in such investigations:

an industry in the United States shall be considered to exist if there is in the United States, with respect to the articles protected by the . . . patent . . . concerned –

(A) significant investment in plant and equipment;

⁷² 19 U.S.C. § 1337(a)(2).

⁷³ *Certain Dynamic Random Access Memories, Components Thereof and Products Containing Same*, Inv. No. 337-TA-242, U.S.I.T.C. Pub. No. 2034 (November 1987), Commission Opinion at 61, 1987 WL 450856 (U.S.I.T.C., September 21, 1987) (“*Certain DRAMs*”).

⁷⁴ *Id.* at 62 (footnotes omitted).

(B) significant employment of labor or capital; or

(C) substantial investment in its exploitation, including engineering, research and development, or licensing.⁷⁵

As the statute uses the disjunctive term “or,” a complainant can demonstrate this so-called “economic prong” of the domestic industry requirement by satisfying any one of the three tests set forth in Section 337(a)(3).⁷⁶ The complainant bears the burden of establishing that the domestic industry requirement is satisfied.⁷⁷

In addition to meeting the economic criteria of the domestic industry requirement, a complainant in a patent-based Section 337 investigation must also demonstrate that it is practicing or exploiting the patents at issue.⁷⁸ In order to find the existence of a domestic industry exploiting a patent at issue, it is sufficient to show that the domestic industry practices any claim of that patent, not necessarily an asserted claim of that patent.⁷⁹ Fulfillment of this so-called “technical prong” of the domestic industry requirement is not determined by a rigid formula, but rather by the articles of commerce and the realities of the marketplace.⁸⁰

⁷⁵ 19 U.S.C. § 1337(a)(3).

⁷⁶ See *Certain Plastic Encapsulated Integrated Circuits*, Inv. No. 337-TA-315, U.S.I.T.C. Pub. No. 2574 (November 1992), Initial Determination at 83, 1992 WL 813952 (U.S.I.T.C., October 15, 1991) (unreviewed by Commission in relevant part) (“*Certain Encapsulated Circuits*”).

⁷⁷ See *Certain Set-Top Boxes and Components Thereof*, Inv. No. 337-TA-454, U.S.I.T.C. Pub. No. 3564 (November 2002), Initial Determination at 294, 2002 WL 31556392 (U.S.I.T.C., June 21, 2002), *unreviewed by Commission in relevant part*, Commission Opinion at 2 (August 29, 2002) (“*Certain Set-Top Boxes*”).

⁷⁸ See 19 U.S.C. § 1337(a)(2) and (3); also see *Certain Microsphere Adhesives, Process for Making Same, and Products Containing Same, Including Self-Stick Repositionable Notes*, Inv. No. 337-TA-366, Commission Opinion at 8, 1996 WL 1056095 (U.S.I.T.C., January 16, 1996) (“*Certain Microsphere Adhesives*”), *aff’d sub nom. Minnesota Mining & Mfg. Co. v. U.S. Int’l Trade Comm’n*, 91 F.3d 171 (Fed. Cir. 1996) (Table); *Certain Encapsulated Circuits*, Commission Opinion at 16.

⁷⁹ *Certain Microsphere Adhesives*, Commission Opinion at 7-16.

⁸⁰ *Certain Diltiazem Hydrochloride and Diltiazem Preparations*, Inv. No. 337-TA-349, (continued...)

The test for claim coverage for the purposes of the technical prong of the domestic industry requirement is the same as that for infringement.⁸¹ “First, the claims of the patent are construed. Second, the complainant’s article or process is examined to determine whether it falls within the scope of the claims.”⁸² As with infringement, the first step of claim construction is a question of law, whereas the second step of comparing the article to the claims is a factual determination.⁸³ To prevail, the patentee must establish by a preponderance of the evidence that the domestic product practices one or more claims of the patent either literally or under the doctrine of equivalents.⁸⁴

D. Validity

A patent is presumed valid.⁸⁵ The party challenging a patent’s validity has the burden of overcoming this presumption by clear and convincing evidence.⁸⁶ Since the claims of a patent measure the invention at issue, the claims must be interpreted and given the same meaning for purposes of both validity and infringement analyses. As with an infringement analysis, an analysis of invalidity involves two steps: the claim scope is first determined, and then the properly construed claim is compared with the prior art to determine whether the claimed invention is anticipated and/or

⁸⁰(...continued)

U.S.I.T.C. Pub. No. 2902, Initial Determination at 138, 1995 WL 945191 (U.S.I.T.C., February 1, 1995) (unreviewed in relevant part) (“*Certain Diltiazem*”); *Certain Double-Sided Floppy Disk Drives and Components Thereof*, Inv. No. 337-TA-215, 227 U.S.P.Q. 982, 989 (Commission Opinion 1985) (“*Certain Floppy Disk Drives*”).

⁸¹ *Certain Doxorubicin and Preparations Containing Same*, Inv. No. 337-TA-300, Initial Determination at 109, 1990 WL 710463 (U.S.I.T.C., May 21, 1990) (“*Certain Doxorubicin*”), *aff’d*, Views of the Commission at 22 (October 31, 1990).

⁸² *Id.*

⁸³ *Markman*, 52 F.3d at 976.

⁸⁴ *See Bayer*, 212 F.3d at 1247.

⁸⁵ 35 U.S.C. § 282; *Richardson-Vicks Inc. v. Upjohn Co.*, 122 F.3d 1476, 1480 (Fed. Cir. 1997) (“*Richardson-Vicks*”).

⁸⁶ *Richardson-Vicks Inc., supra*; *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044 (Fed. Cir.) (“*Uniroyal*”), *cert. denied*, 488 U.S. 825 (1988).

rendered obvious.⁸⁷

1. Anticipation, 35 U.S.C. §§ 102 (a), (b) and (e)

A patent may be found invalid as anticipated under 35 U.S.C. § 102(a) if “the invention was known or used by others in this country, or patented or described in a printed publication in this country, or patented or described in a printed publication in a foreign country, before the invention thereof by the applicant for patent.” 35 U.S.C. § 102(a). A patent may be found invalid as anticipated under 35 U.S.C. § 102(b) if “the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States.”⁸⁸ Under 35 U.S.C. § 102(e), a patent is invalid as anticipated if “the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent.”⁸⁹ Anticipation is a question of fact.⁹⁰

Under the foregoing statutory provision, a claim is anticipated and therefore invalid when “the four corners of a single, prior art document describe[s] every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation.”⁹¹ To be considered anticipatory, the prior art reference must be enabling and describe the applicant’s claimed invention sufficiently to have placed it in

⁸⁷ *Amazon.com, Inc. v. Barnesandnoble.com, Inc.*, 239 F.3d 1343, 1351 (Fed. Cir. 2001) (“*Amazon.com*”).

⁸⁸ 35 U.S.C. § 102(b).

⁸⁹ 35 U.S.C. § 102(e).

⁹⁰ *Texas Instruments, Inc. v. U.S. Int’l Trade Comm’n*, 988 F.2d 1165, 1177 (Fed. Cir. 1993) (“*Texas Instruments IP*”).

⁹¹ *Advanced Display Sys., Inc. v. Kent State Univ.*, 212 F.3d 1272, 1282 (Fed. Cir. 2000), *cert. denied*, 532 U.S. 904 (2001) (“*Advanced Display Systems*”).

possession of a person of ordinary skill in the field of the invention.⁹² But, the degree of enabling detail contained in the reference does not have to exceed that contained in the patent at issue.⁹³

Further, the disclosure in the prior art reference does not have to be express, but may anticipate by inherency where the inherency would be appreciated by one of ordinary skill in the art.⁹⁴ To be inherent, the feature must necessarily be present in the prior art.⁹⁵ Inherency may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. If, however, the disclosure is sufficient to show that the natural result flowing from the operation as taught would result in the performance of the questioned function, it seems to be well settled that the disclosure should be regarded as sufficient. This modest flexibility in the rule that "anticipation" requires that every element of the claims appear in a single reference accommodates situations where the common knowledge of technologists is not recorded in the reference; that is, where technological facts are known to those in the field of the invention, albeit not known to judges.⁹⁶

2. Obviousness, 35 U.S.C. § 103 (a)

Under 35 U.S.C. § 103(a), a patent is valid unless "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

⁹² *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F.3d 1339, 1346 (Fed. Cir. 2000) ("*Helifix*"); *In re Paulsen*, 30 F.3d 1475, 1478 (Fed. Cir. 1994) ("*Paulsen*").

⁹³ *Paulsen*, 30 F.3d at 1481 n.9.

⁹⁴ *Glaxo Inc. v. Novopharm Ltd.*, 52 F.3d 1043, 1047 (Fed. Cir.), *cert. denied*, 516 U.S. 988 (1995) ("*Glaxo*").

⁹⁵ See *Finnigan Corp. v. U.S. Int'l Trade Comm'n*, 180 F.3d 1354, 1365-66 (Fed. Cir. 1999) ("*Finnigan*").

⁹⁶ See *Cont'l Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268-69 (Fed. Cir. 1991) ("*Continental Can*"); *Finnigan*, 180 F.2d at 1365.

subject matter pertains.”⁹⁷ The ultimate question of obviousness is a question of law, but “it is well understood that there are factual issues underlying the ultimate obviousness decision.”⁹⁸

Once claims have been properly construed, “[t]he second step in an obviousness inquiry is to determine whether the claimed invention would have been obvious as a legal matter, based on underlying factual inquiries including : (1) the scope and content of the prior art, (2) the level of ordinary skill in the art, (3) the differences between the claimed invention and the prior art ; and (4) secondary considerations of non-obviousness” (also known as “objective evidence”).⁹⁹

Although the Federal Circuit case law also required that, in order to prove obviousness, the patent challenger must demonstrate, by clear and convincing evidence, that there is a “teaching, suggestion, or motivation to combine, the Supreme Court has rejected this “rigid approach” employed by the Federal Circuit in *KSR Int’l Co. v. Teleflex Inc.*:¹⁰⁰

When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Sakraida and Anderson’s-Black Rock are illustrative—a court must ask whether the improvement is more than the predictable use of prior art elements according to their established function.

Following these principles may be more difficult in other cases than it is here because the claimed subject matter may involve more than the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement. Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known

⁹⁷ 35 U.S.C. § 103(a).

⁹⁸ *Richardson-Vicks Inc.*, 122 F.3d at 1479; *Wang Lab., Inc. v. Toshiba Corp.*, 993 F.2d 858, 863 (Fed. Cir. 1993) (“*Wang Laboratories*”).

⁹⁹ *Smiths Indus. Med. Sys., Inc. v. Vital Signs, Inc.*, 183 F.3d 1347, 1354 (Fed. Cir. 1999) (“*Smiths Industries*”), citing *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966) (“*Graham*”).

¹⁰⁰ *KSR Int’l Co. v. Teleflex Inc.*, 500 U.S. – (2007), 127 S.Ct. 1727, 1739 (“*KSR*”).

to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. To facilitate review, this analysis should be made explicitly. See *In re Kahn*, 441 F.3d 977, 988 (CA Fed. 2006) (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusions of obviousness”). As our precedents make clear, however, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

[...]

The obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents. The diversity of inventive pursuits and of modern technology counsels against limiting the analysis in this way. In many fields it may be that there is little discussion of obvious techniques or combinations, and it often may be the case that market demand, rather than scientific literature, will drive design trends. Granting patent protection to advance that would occur in the ordinary course without real innovation retards progress and may, in the case of patents combining previously known elements, deprive prior inventions of their value or utility.¹⁰¹

“Secondary considerations,” also referred to as “objective evidence of non-obviousness,” such as “commercial success, long felt but unsolved needs, failure of others, etc.” may be used to understand the origin of the subject matter at issue, and may be relevant as indicia of obviousness or non-obviousness.¹⁰² Secondary considerations may also include copying by others, prior art teaching away, and professional acclaim.¹⁰³

¹⁰¹ *KSR*, 500 U.S. at – ; 127 S.Ct. at 1740-41.

¹⁰² *Graham*, 383 U.S. at 17-18.

¹⁰³ See *Perkin-Elmer Corp. v. Computervision Corp.*, 732 F.2d 888, 894 (Fed. Cir. 1984) (“*Perkin-Elmer*”), cert. denied, 469 U.S. 857 (1984); *Avia Group Int’l, Inc. v. L.A. Gear California*, 853 F.2d 1557, 1564 (Fed. Cir. 1988) (“*Avia*”) (copying by others); *In re Hedges*, 783 F.2d 1038, 1041 (Fed. Cir. 1986) (“*Hedges*”) (prior art teaching away; invention contrary to accepted wisdom); *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565 (Fed. Cir. 1986) (“*Kloster*”), cert. denied, 479 (continued...)

Evidence of “objective indicia of non-obviousness,” also known as “secondary considerations,” must be considered in evaluating the obviousness of a claimed invention, but the existence of such evidence does not control the obviousness determination. A court must consider all of the evidence under the *Graham* factors before reaching a decision on obviousness.¹⁰⁴ In order to accord objective evidence substantial weight, its proponent must establish a nexus between the evidence and the merits of the claimed invention, and a *prima facie* case is generally made out “when the patentee shows both that there is commercial success, and that the thing (product or method) that is commercially successful is the invention disclosed and claimed in the patent.”¹⁰⁵ Once the patentee has made a *prima facie* case of nexus, the burden shifts to the challenger to show that the commercial success was caused by “extraneous factors other than the patented invention, such as advertising, superior workmanship, etc.”¹⁰⁶

3. Written Description/Enablement, 35 U.S.C. § 112, ¶ 1

Section 112, ¶ 1 of Title 35 requires that the specification describe the manner and process of making and using the invention “in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same.”

¹⁰³(...continued)

U.S. 1034 (1987) (wide acceptance and recognition of the invention).

¹⁰⁴ *Richardson-Vicks Inc.*, 122 F.3d at 1483-84.

¹⁰⁵ *In re GPAC Inc.*, 57 F.3d 1573, 1580 (Fed. Cir. 1995) (“GPAC”); *Demaco Corp. v. F. Von Langsdorff Licensing Ltd.*, 851 F.2d 1387, 1392 (Fed. Cir. 1988), *cert. denied*, 488 U.S. 956 (1988) (“Demaco”); *Certain Crystalline Cefadroxil Monohydrate*, Inv. No. 337-TA-293, Commission Opinion (March 15, 1990), 15 U.S.P.Q.2d 1263, 1270 (“*Certain Crystalline*”).

¹⁰⁶ *Id.* at 1393.

The issue of whether a disclosure is enabling is a matter of law.¹⁰⁷ “To be enabling, the specification of a patent must teach those skilled in the art how to make and use the full scope of the claimed invention without ‘undue experimentation.’”¹⁰⁸ “Patent protection is granted in return for an enabling disclosure of an invention, not for vague, intimations of general ideas that may or may not be workable.”¹⁰⁹ Although a specification need not disclose minor details that are well known in the art, “[i]t is the specification, not the knowledge of one skilled in the art, that must supply the novel aspects of an invention in order to constitute adequate enablement,” and in so doing the specification cannot merely provide “only a starting point, a direction for further research.”¹¹⁰ On the other hand, “[i]t is not fatal if some experimentation is needed, for the patent document is not intended to be a production specification.”¹¹¹ “Undue experimentation” is “a matter of degree” and “not merely quantitative, since a considerable amount of experimentation is permissible, if it is merely routine, or if the specification in question provides a reasonable amount of guidance with respect to the direction in which the experimentation should proceed”¹¹²

It is well-settled that in order to be enabling under Section 112, “the patent must contain a description sufficient to enable one skilled in the art to make and use the full scope of the claimed

¹⁰⁷ *Applied Materials, Inc. v. Advanced Semiconductor Materials America, Inc.*, 98 F.3d 1563, 1575 (Fed. Cir. 1996) (“*Applied Materials*”).

¹⁰⁸ *Genentech, Inc. v. Novo Nordisk, A/S*, 108 F.3d 1361, 1365 (Fed. Cir. 1997) (“*Genentech*”).

¹⁰⁹ *Id.* at 1366.

¹¹⁰ *Id.*

¹¹¹ *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 941 (Fed. Cir. 1990) (“*Northern Telecom*”).

¹¹² *PPG Industries, Inc. v. Guardian Industries Corp.*, 75 F.3d 1558, 1564 (Fed. Cir. 1996) (“*PPG Industries*”).

invention.”¹¹³ Section 112 requires that the scope of the claims must bear a reasonable correlation to the scope of enablement provided by the specification to such persons.¹¹⁴

E. Enforceability

1. Inequitable Conduct

A patent is unenforceable on grounds of “inequitable conduct” if the patentee withheld material information from the PTO with intent to mislead or deceive the PTO into allowing the claims.¹¹⁵ Both materiality and intent must be proven by clear and convincing evidence.¹¹⁶ When inequitable conduct occurs in relation to one or more claims of a patent, the entire patent is unenforceable.¹¹⁷

According to the rules of the PTO, the duty to disclose information “exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim.”¹¹⁸

Generally, when withheld information is highly material, a lower showing of deceptive intent

¹¹³ *United States v. Teletronics, Inc.*, 857 F.2d 778, 785 (Fed. Cir. 1988) (“*Teletronics*”); see also *Amgen, Inc. v. Chugai Pharmaceutical Co., Ltd.*, 927 F.2d 1200, 1213 (Fed. Cir. 1991) (“*Chugai*”) (inventor’s disclosure must be “sufficient to enable on skilled in the art to carry out the invention commensurate with the scope of his claims”).

¹¹⁴ *Application of Fischer*, 427 F.2d 833, 839 (C.C.P.A. 1970) (“*Fischer*”).

¹¹⁵ *LaBounty Mfr., Inc. v. U.S. Int’l Trade Comm’n*, 958 F.2d 1066, 1070-1074 (Fed. Cir. 1992) (“*LaBounty*”).

¹¹⁶ *Id.*; *Kingsdown Med. Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 872 (Fed. Cir. 1988), cert. denied, 490 U.S. 1067 (1989) (“*Kingsdown*”).

¹¹⁷ *Kingsdown*, 863 F.2d at 874.

¹¹⁸ 37 C.F.R. § 1.56(a).

will be sufficient to establish inequitable conduct.¹¹⁹ Moreover, “[d]irect proof of wrongful intent is rarely available but may be inferred from clear and convincing evidence of the surrounding circumstances.”¹²⁰ The conduct at issue must be viewed in light of all the evidence, including evidence of good faith.¹²¹ In other words “where withheld information is material and the patentee knew or should have known of that materiality, he or she can expect to have great difficulty in establishing subjective good faith sufficient to overcome an inference of intent to mislead.”¹²²

“Information is material where there is a substantial likelihood that a reasonable examiner would consider it important in deciding whether to allow the application to issue as a patent.”¹²³ A patent applicant, however, has no obligation to disclose a reference that is cumulative or less pertinent than those already before the examiner.¹²⁴ Under the rules of the PTO, information is material when it is not cumulative to information of record and it either (i) “establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim”; or (ii) “it refutes, or is inconsistent with, a position the applicant takes” in either opposing the PTO’s argument of unpatentability or asserting the applicant’s own argument of patentability.¹²⁵ Close cases,

¹¹⁹ *Am. Hoist & Derrick Co. v. Sowa & Sons, Inc.*, 725 F.2d 1350, 1363 (Fed. Cir.), *cert. denied*, 469 U.S. 821 (1984) (“*American Hoist*”).

¹²⁰ *LaBounty*, 958 F.2d at 1076; *Bristol-Myers Squibb Co. v. Rhone-Poulenc Rorer, Inc.*, 326 F.3d 1226, 1239 (Fed. Cir. 2003) (“*Bristol-Myers*”); *GFI*, 265 F.3d at 1274; *Merck & Co. v. Danbury Pharmacal, Inc.*, 873 F.2d 1418, 1422 (Fed. Cir. 1989) (“*Danbury*”).

¹²¹ *Kingsdown*, 863 F.2d at 876.

¹²² *Bristol-Myers Squibb*, 326 F.3d at 1239 (citing *Akron Polymer Container Corp. v. Exxel Container, Inc.*, 148 F.3d 1380, 1384 (Fed. Cir. 1998) (“*Akron*”)); *see also GFI*, 265 F.3d at 1275.

¹²³ *LaBounty*, 958 F.2d at 1074; *GFI*, 265 F.3d at 1274; *Molins PLC v. Textron, Inc.*, 48 F.3d 1172, 1179 (Fed. Cir. 1995) (“*Molins*”).

¹²⁴ *Halliburton Co. v. Schlumberger Tech. Corp.*, 925 F.2d 1435, 1439-40 (Fed. Cir. 1991) (“*Halliburton*”).

¹²⁵ 37 C.F.R. § 1.56(b).

however, “should be resolved by disclosure, not unilaterally by applicant.”¹²⁶

2. Improper Inventorship, 35 U.S.C. § 102(f)

The patent statute provides that when an invention is made by two or more persons, they shall apply for the patent jointly.¹²⁷ Where there is joint inventorship, the patent must issue to all inventors.¹²⁸

The issuance of a patent creates a presumption that the named inventors are the true and only inventors.¹²⁹ “In order to rebut this presumption, a party challenging patent validity for omission of an inventor must present clear and convincing evidence that the omitted individual actually invented the claimed invention.”¹³⁰ Inventorship is a question of law.¹³¹

“Conception is the touchstone of inventorship.”¹³² It is the “formation in the mind of the inventor, of a definite and permanent idea of the complete and operative invention as it is hereafter to be applied in practice.”¹³³ “An idea is sufficiently ‘definite and permanent’ when ‘only ordinary skill would be necessary to reduce the invention to practice, without extensive research or

¹²⁶ *Abbott Laboratories v. TorPharm, Inc.*, 300 F.3d 1367, 1379 (Fed. Cir. 2002) (“*TorPharm*”) quoting *LaBounty*, 958 F.2d at 1076.

¹²⁷ 35 U.S.C. § 116; also see *Certain EPROM, EEPROM, Flash Memory, and Flash Microcontroller Semiconductor Devices, and Products Containing Same*, Inv. No. 337-TA-395, USITC Pub. No. 3136, Commission Opinion at 7 (October 1998) (“*Certain EPROM*”).

¹²⁸ 35 U.S.C. §§ 102(f), 116, and 256.

¹²⁹ *Ethicon, Inc. v. United States Surgical Corp.*, 135 F.3d 1456, 1460 (Fed.Cir.), *cert. denied*, 525 U.S. 923 (1998) (“*Ethicon II*”).

¹³⁰ See *Acromed*, 253 F.3d at 137.

¹³¹ *Ethicon II*, *supra*.

¹³² *Burroughs Wellcome Co. v. Barr Laboratories, Inc.*, 40 F.3d 1223, 1227 (Fed.Cir. 1994), *cert. denied*, 516 U.S. 1070 (1996) (“*Burroughs*”).

¹³³ *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1376 (Fed.Cir. 1986) (“*Hybritech*”).

experimentation.”¹³⁴ “The conceived invention must include every feature of the subject matter claimed in the patent.”¹³⁵ Moreover, in the case of patent claims having means-plus-function language, “the contributor of any disclosed means of a means-plus-function claim element is a joint inventor as to that claim, unless one asserting sole inventorship can show that the contribution of that means was simply a reduction to practice of the sole inventor’s broader concept.”¹³⁶

To be a joint inventor, “an individual must make a contribution to the conception of the claimed invention that is not insignificant in quality, when that contribution is measured against the dimension of the full invention.”¹³⁷ Each of the joint inventors, however, does not have to make the same type or amount of contribution to the invention; each needs to perform only a part of the task which produces the invention.¹³⁸ Further, a co-inventor need not make a contribution to every claim of a patent; a contribution to one claim is enough.¹³⁹ “Thus, the critical question for joint conception is who conceived, as that term is used in the patent law, the subject matter of the claims at issue.”¹⁴⁰

A person does not qualify as a joint inventor by merely assisting the actual inventor after conception of the claimed invention.¹⁴¹ “One who simply provides the inventor with well-known principles or explains the state of the art without ever having ‘a firm and definite idea’ of the claimed combination as a whole does not qualify as a joint inventor.”¹⁴²

In order to be considered a joint inventor, there must be clear and convincing evidence

¹³⁴ *Ethicon II, supra*, 135 F.3d at 1460.

¹³⁵ *Id.*

¹³⁶ *Id.* at 1463; quoted in *Certain EPROM, supra*.

¹³⁷ *Fina Oil & Chemical Co. v. Ewen*, 123 F.3d 1466, 1473 (Fed.Cir. 1997) (“*Fina*”).

¹³⁸ *Ethicon II, supra*.

¹³⁹ *Id.*

¹⁴⁰ *Id.*

¹⁴¹ *Id.*

¹⁴² *Id.*

corroborating the individual's contribution.¹⁴³ In *Ethicon II*, the Federal Circuit noted in this regard that:

an inventor's testimony respecting the facts surrounding a claim of derivation or priority of invention cannot, standing alone, rise to the level of clear and convincing proof. *Price v. Symsek*, 988 F.2d 1187, 1194, 26 USPQ2d 1031, 1036 (Fed.Cir. 1993). The rule is the same for an alleged co-inventor's testimony. *See Hess*, 106 F.3d at 980. Thus, an alleged co-inventor must supply evidence to corroborate his testimony. *See Price*, 988 F.2d at 1194. Whether the inventor's testimony has been sufficiently corroborated is evaluated under a "rule of reason" analysis. *Id.* at 1195. Under this analysis, "[a]n evaluation of all pertinent evidence must be made so that a sound determination of the credibility of the [alleged] inventor's story may be reached." *Id.*

Corroborating evidence may take many forms. Often contemporaneous documents prepared by a putative inventor serve to corroborate an inventor's testimony. *See id.* at 1195-96. Circumstantial evidence about the inventive process may also corroborate. *See Knorr v. Pearson*, 671 F.2d 1368, 1373, 213 USPQ 196, 200 (CCPA 1982) ("[S]ufficient circumstantial evidence of an independent nature can satisfy the corroboration rule.") Additionally, oral testimony of someone other than the alleged inventor may corroborate. *See Price*, 988 F.2d at 1195-96.¹⁴⁴

IV. The '338 Patent

As stated earlier, the '338 patent has been litigated by SanDisk at the ITC on two previous occasions, making this investigation the third time SanDisk has asserted the '338 patent in front of three different presiding Administrative Law Judges. Based on the evidence presented in this investigation, the undersigned finds that it is unnecessary to perform a complete analysis of the '338 patent yet again¹⁴⁵ because an analysis of SanDisk's economic prong for domestic industry will be

¹⁴³ *Fina, supra*, 123 F.3d at 1474.

¹⁴⁴ *Ethicon II, supra*, 135 F.3d at 1461; quoted in *Certain EPROM*, Initial Determination at 97-98 (March 19, 1998, Public version April 29, 1998).

¹⁴⁵ Even if the undersigned were to do a complete analysis of the '338 patent, the undersigned previously stated, during the prehearing conference that,

I did want to mention, though, I meant to mention this at the beginning, and I believe it's related somewhat to this matter here. We're talking about, again, the 526

(continued...)

sufficient to show that there can be no relief for SanDisk regarding the '338 patent because SanDisk's evidence falls significantly below the standard of meeting their "preponderance of the evidence" burden.¹⁴⁶

While it has been customary for administrative law judges to address all outstanding issues in their initial determinations, the undersigned finds that this is an appropriate case where it would be a waste of judicial resources to go through a complete analysis of claim construction, infringement, domestic industry technical prong, validity, and enforceability, when it is clear that the economic prong of domestic industry has not been met, and when the Complainant has litigated the case at the Commission twice before.

ST takes issue with SanDisk's timing of the filing of the Complaint in this investigation,¹⁴⁷

¹⁴⁵(...continued)

proceeding, which, as the parties have indicated, is currently before the Federal Circuit. I understand the maxim of administrative law that nothing is ever set in stone, at least when a new case is filed, and that I am free to revisit matters in this case. However, it is my intention to adopt the Commission's claim construction to the extent it was decided in the 526 proceeding for purposes of this case. And this is a fairly recent case. I don't see any need to revisit that. I understand that I'm free to do that. But given the circumstances, unless someone can really show me some reason why I should deviate from what the Commission has already decided, I'm not going to do that.

Bullock, Tr. 20 (12/01/06).

¹⁴⁶ See *Certain Encapsulated Integrated Circuit Devices and Products Containing Same*, Inv. No. 337-TA-501 (Remand), Initial Determination at 102 (Nov. 9, 2005) ("*Certain Encapsulated Integrated Circuits*") ("The burden of showing something by a 'preponderance of the evidence' . . . simply requires the trier of fact to believe that the existence of a fact is more probable than its nonexistence before [he] may find in favor of the party who the burden to persuade the [judge] of the fact's existence.")

¹⁴⁷ See RIB 1 ("SanDisk acted in haste. Barely a month after the Commission affirmed Judge Luckern's ruling in 337-TA-526 that ST's and SanDisk's NAND products do not practice the means-plus-function limitations of the then-asserted '338 claims, SanDisk filed again. In this second consecutive action against ST in under 15 months, SanDisk reasserted the '338 patent, and added the '517 and '956 patents for good measure. SanDisk's haste made waste.")

which was just thirty-five days after the Commission determined to affirm Judge Luckern's determination of non-infringement of the '338 patent, which was subsequently affirmed by the Federal Circuit.¹⁴⁸ This may or may not be the basis for the inadequacy of SanDisk's presentation on the economic prong. Therefore, the timing of the filing of the Complaint, in and of itself, is not the basis for the undersigned's ruling on this matter. As has already been discussed in the undersigned's previous orders, SanDisk was relying on Intel, a licensee, for its domestic industry in the '338 patent. Yet SanDisk never contacted Intel before it filed the Complaint in this investigation. While there is no requirement for SanDisk to have contacted Intel before filing the Complaint, it would have been in SanDisk's best interest to do so, which was already discussed at length in Order No. 21.¹⁴⁹

To make matters worse, SanDisk took inconsistent positions regarding proving its case for economic prong for the '338 patent. In SanDisk's pleadings to the undersigned regarding the motion to enforce the subpoena against Intel, SanDisk represented to the undersigned, along with the other parties in this investigation, that SanDisk was relying "solely" on Intel's practice of the '338 patent for domestic industry. Yet, when the undersigned denied the motion to enforce the subpoena against Intel, SanDisk reverted back to its position that it would rely on its own licensing activities to prove domestic industry.¹⁵⁰ While SanDisk attempted to explain away the inconsistency by claiming they were regrettably litigating on "two parallel paths," the undersigned ruled that counsel should be held accountable to the statements made in their motions, and that SanDisk should be limited to relying only on Intel's practice of the '338 patent:

¹⁴⁸ See *SanDisk, supra*.

¹⁴⁹ See also Order No. 26.

¹⁵⁰ See generally, Tr. 99-124 (12/01/06), 134-162 (12/04/06).

To me if you wanted to keep your options open, you should have said this – for example, this is one of the main bases for – that we're going to be relying on for domestic industry. But to make a kind of unqualified statement here and then say, well, we didn't really mean that. I mean I guess it's – at a certain point I have to be able to rely on statements. I mean, I guess what you're saying is, well, it was our sole basis but it really wasn't our sole basis. I have a problem with that.¹⁵¹

[...]

This is something that I'm sure everyone who deals in this practice here at the Commission, the 337 practice, it's very fast track. It's very precise. We have rules that are much stricter – let's say, I've been at other administrative agencies where we haven't had these rules. But the fact that we are required, we the judges and the Commission are required to get these cases out as much as practical within the 18-month period, we have to have very strict rules. Here we have a case where it's complainant, this is the third time you've been here. I realize the facts are somewhat different. But complainant has some advantage in the sense they can pick the timing of the case. And the assumption is that, when complainant comes here, they are ready to go. They've gotten their – all of the discovery they need, at least from, let's say from Intel, if you're going to be relying on Intel, that's one example. And I come back again to the argument of the statements made to – made to the judge. I think these are very unequivocal statements. I understand there's some ambiguity here. But just as if someone fails to raise an issue in an expert report, and that expert is precluded from testifying, those are the rules. This is a highly specialized practice. And I think when you miss – when a mistake is made, the question is, it should – it seems to me, it should be upon the person who made the mistake. And I'm not saying it was a willful error. But it was one nonetheless. And I think I, and the others, have a right to rely on the statement that was made that complainant was relying on licensing with respect to Intel. So my ruling from Friday stands.¹⁵²

The ruling was that SanDisk was prohibited from using its own licensing activities as an alternate basis for proving economic prong of domestic industry in light of statements of counsel that Intel's practice of the '338 patent would be the *sole basis* for SanDisk's case for meeting the economic prong requirement. SanDisk then commissioned a report from Semico–CX-481–to prove Intel's domestic industry in the '338 patent. As discussed below, however, the Semico report is

¹⁵¹ Bullock, Tr. 121 (12/01/06).

¹⁵² Bullock, Tr. 160-62 (12/04/06).

based on nothing more than assumptions, guesses, and estimates, making it wholly unreliable and therefore entitled to no weight. Further, any testimony that relies solely on the Semico report is also entitled to no weight, *i.e.* CX-2234C (Napper Direct); CX-2296C (Napper Rebuttal).

SanDisk asserts that the economic prong of the domestic industry requirement for the '338 patent is satisfied under 19 U.S.C. § 1337(a)(3)(A), (B), and (C) because Intel, a licensee of the '338 patent, has made significant investment in plant and equipment, significant employment of labor or capital, and made a substantial investment in R&D and engineering related to the '338 patent.¹⁵³

According to SanDisk, Intel has manufactured and sold its StrataFlash (MLC NOR) line of products since 1997 and has sold 100 million L18/L30 StrataFlash between Q3-Q4 of 2003 and 1 billion flash memory chips by 2000 and 2 billion flash memory chips by 2003.¹⁵⁴ According to SanDisk, Intel's 130 nm, 180 nm, and 250 nm NOR MLC (StrataFlash) products all practice the '338 patent.¹⁵⁵ SanDisk asserts that Intel has a fabrication facility in New Mexico that is used for manufacturing flash memory. SanDisk asserts that approximately 37%, 69%, 78%, and 64% of the revenue of all the flash memory manufactured at Intel's New Mexico fab in 2002, 2003, 2004, and 2005, respectively, is attributable to the 130 nm, 180 nm, and 250 nm MLC NOR chips.¹⁵⁶

Specifically, SanDisk asserts that, for 2005, Intel had a \$4.3 million investment in domestic plant and equipment related to the 130 nm, 180 nm, and 250 nm StrataFlash. This is based on a "conservative estimation," based on Intel's total investment of \$11-\$12 billion in net property, plant

¹⁵³ CIB 59.

¹⁵⁴ CIB 59-60 citing CX-436 (Intel news release, 9/26/01); CX-437 (Intel news release, 4/10/03); CX-439 (Intel news release 5/22/00); CX-481C (Semico Report); CX-2234C (Napper Direct) at Q. 87-88.

¹⁵⁵ CIB 60 citing CX-2229C (Rhyne Direct) at Q. 1324-1404.

¹⁵⁶ CIB 60 citing CX-363 (Intel 10K); CX-481C (Semico Report); CX-2234C (Napper Direct) at Q. 107-13.

and equipment in the U.S. from 2003-2005.¹⁵⁷ SanDisk asserts that, between 2003 and 2005, Intel employed approximately 1700-2600 people to work in the U.S. related to the 130 nm, 180 nm, and 250 nm StrataFlash.¹⁵⁸ SanDisk asserts that, between 2003 and 2004, Intel invested approximately \$200 million in domestic R&D and engineering related to the 130 nm, 180 nm, and 250 nm StrataFlash.¹⁵⁹

ST asserts that SanDisk's domestic industry evidence is unreliable because there is no direct evidence from Intel regarding its U.S. economic activities related to the 130 nm, 180 nm, and 250 nm StrataFlash. ST asserts that the only evidence provided by SanDisk is a third party report¹⁶⁰ that is full of second-hand information, estimates, and unfounded assumptions, consisting of spreadsheets and document fragments with no narrative explanation or supporting witness testimony, which is completely unreliable and should be entitled to no weight. ST asserts that, as of matter of fact or policy, SanDisk's evidence should be rejected as insufficient to establish its legal standing to maintain this action on behalf of the purported "domestic industry." According to ST, the author of the Semico report was never produced for questioning regarding the sources used, or the assumptions made. Therefore, there is no way to verify the reliability of the estimates made. ST also asserts that SanDisk's reliance on its expert, Mr. Napper, is also unreliable because Mr. Napper relied on the numbers presented within the Semico report. Furthermore, ST notes that Mr. Napper made a

¹⁵⁷ CIB 60 citing CX-363 (Intel 10K); CX-442 (Intel worldwide manufacturing and assembly test sites at a glance - fabs); CX-481C (Semico Report); CX-2234C (Napper Direct) at Q. 96, 102-06, 113; Napper, Tr. 911.

¹⁵⁸ CIB 61 citing CX-363 (Intel 10K); CX-364 (Intel 10K); CX-481C (Semico Report); CX-600 (Intel 10K); CX-2234C (Napper Direct) at Q. 121-22; Napper, Tr. 911.

¹⁵⁹ CIB 61 citing CX-363 (Intel 10K); CX-380 (Intel presentation - continuing Moore's law cost reduction in non volatile semiconductor memories); CX-481C (Semico Report); CX-2234C (Napper Direct) at Q. 114, 116, 120.

¹⁶⁰ CX-481 (Semico Report).

miscalculation in his expert report, which rippled through all of his calculations, making his testimony further unreliable.¹⁶¹

ST asserts that, even if the estimates of Intel's 130 nm manufacturing activities were accepted, SanDisk has not met its burden. According to ST, both the Semico report and Mr. Napper attribute 100% of the cost of manufacturing and employment to Intel's fabrication facilities, ignoring all other production steps. According to ST, the evidence shows that Intel conducts final production of its flash memory chips at assembly and test facilities in the Philippines and China. Therefore, ST asserts that SanDisk should have performed a comparative analysis of the production activities to determine whether the domestic portion is significant, but that SanDisk failed to do so.¹⁶²

ST also asserts that, by April 1, 2007, Intel will have totally withdrawn from producing the domestic industry products. The Semico report shows that Intel discontinued producing the 250 nm in 2002 and the 180 nm in 2004. As for the 130 nm, production will be completely phased out by the second quarter of 2007, when it will be replaced by the 90 nm, which SanDisk does not allege to practice the '338 patent.¹⁶³ According to ST, voluntary withdrawal from the market eliminates the required domestic industry and extinguishes the need for a remedial order.¹⁶⁴

Staff asserts that the publicly available information, relied upon by SanDisk, is insufficient to allow SanDisk to meet its burden of proof regarding the economic prong for the '338 patent. According to Staff, based on the evidence in the record, a preponderance of the evidence does not

¹⁶¹ RIB 58-59; RRB 22-23.

¹⁶² RIB 59 citing *Certain Microlithographic Machines and Components Thereof*, Inv. No. 337-TA-468, Initial Determination at 347-52 (January 29, 2003) ("*Certain Microlithographic Machines*").

¹⁶³ RIB 60 citing CDX-II-155; RFF2315-17.

¹⁶⁴ RIB 60 citing *Certain Variable Speed Wind Turbines*, Inv. No. 337-TA-376, Comm'n Op. at 26 (September 23, 1996) ("*Certain Wind Turbines*").

show how much Intel has invested in the United States related to the 130 nm, 180 nm, and 250 nm StrataFlash, and whether the investment is substantial or significant, as required by Section 337.¹⁶⁵

According to Staff, SanDisk relies exclusively on Intel's investments in plant, equipment, labor, and capital in its New Mexico fab. Staff asserts, however, that Intel has never publicly disclosed the level of its property, plant and equipment allocated to its New Mexico fab, nor how many people are employed in New Mexico, along with what kind of work they do.¹⁶⁶ According to Staff, SanDisk's arguments are based on nothing more than the fact that Intel, at one point in time, produced chips at the New Mexico fab.¹⁶⁷ As for Intel's research and development, SanDisk's analysis is also entirely speculative because there is simply no evidence of where Intel conducted any research and development relating to [] chips.¹⁶⁸

Staff counters ST's argument that it is impossible to base a domestic industry on a product that has been discontinued.¹⁶⁹ According to Staff, whether a domestic industry continues to exist is a factor that may be considered, but the fact that there is no longer any domestic production does not, by itself, indicate that relief is not appropriate.¹⁷⁰ Staff also disagrees that a "comparative analysis" of foreign and domestic investment is required.¹⁷¹

The undersigned finds that SanDisk has failed to meet its burden of proof for the economic prong of domestic industry for the '338 patent. The evidence cited by SanDisk is unreliable and

¹⁶⁵ SIB 60-61; SRB 31-33.

¹⁶⁶ SIB 61 citing CX-2234 (Napper Direct) at 33; Napper, Tr. 1012-13.

¹⁶⁷ SRB 32.

¹⁶⁸ SIB 62 citing Napper, Tr. 948-49; RX-2154C (Mulhern Rebuttal) at 12-13.

¹⁶⁹ SRB 32-33, n. 3.

¹⁷⁰ SRB 33, n. 3 citing *Certain Wind Turbines*, Comm'n Op. at 10-13.

¹⁷¹ SRB 33, n.3 citing *Certain Personal Computers, Server Computers, and Components Thereof*, Inv. No. 337-TA-509, Notice of Commission Determination at 2-3 (April 6, 2005) ("*Certain Personal Computers*").

unpersuasive. SanDisk's relies on estimates and projections from a market research firm hired for this investigation, rather than any concrete figures from Intel regarding these specific accused products. The only concrete numbers obtained from Intel were from its SEC filings, which report figures for total U.S. operations for all of its products.

Because SanDisk did not have any direct evidence from Intel, it hired a third party to put together a report, which was admitted into evidence as CX-481. The Semico Report quite explicitly states that the information contained in the report is based on "Semico's estimate of data not disclosed by Intel."¹⁷² As noted by Staff, "Complainant's methodology is to take a guess, divide it by an estimate, divide it by another estimate, and allocated the final figure based on an assumption."¹⁷³ A calculation that "adds vague estimation and gross extrapolation to unsupported presumption," that "[a]t every step . . . is fraught with speculation," cannot satisfy a party's burden of proof. The undersigned agrees. Because SanDisk has failed to produce any evidence of Intel's domestic industry other than the Semico report, along with the testimony of Mr. Napper, who also relies on the Semico report, SanDisk has failed to prove, by a preponderance of the evidence, that it has met the economic prong of domestic industry for the '338 patent.

Perhaps if SanDisk would have approached Intel before the Complaint was filed, SanDisk would have had the requisite information needed to prove its case, or SanDisk could have determined that Intel did not have a domestic industry in the '338 patent and not have asserted the '338 patent in this investigation. Instead, SanDisk, acting in haste, subjected ST to months of relitigating the '338 patent, wasting both public and private resources. Therefore, no other judicial

¹⁷² CX-481 (Semico Report) at SDITC-II 166601.

¹⁷³ SIB 62.

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¹⁷² CX-481 (Semico Report) at SDITC-II 166601.

¹⁷³ SIB 62.

resources will be consumed in addressing this patent.

V. The '517 Patent

A. Claim Construction

1. Asserted Claims

The asserted claims read as follows (with the first instance of the disputed terms highlighted in *italics*):

1. A method of operating an *EEprom system* having memory cells that individually include an *electrically floating gate* carrying a *charge level that is alterable in response to appropriate voltage conditions being applied to the cell in order to set a variable threshold level thereof into a range that is determinable by reading the cell*, said method comprising:
 - applying said appropriate voltage conditions in parallel to a plurality of said memory cells*, thereby to alter the charge levels on the floating gates of said plurality of memory cells,
 - determining the threshold level ranges in which individual ones of said plurality of memory cells lie*, and
 - terminating said application of appropriate voltage conditions to individual ones of said plurality of memory cells upon their being determined to have reached desired threshold level ranges while continuing to apply said appropriate voltage conditions to others of said plurality of cells until all of the plurality of cells are determined to have reached their desired threshold level ranges.*
3. The method of claim 1, wherein there are more than two threshold level ranges.
5. The method of claim 1, wherein the threshold level ranges are separated by more than one *breakpoint threshold level*, thereby to provide more than two non-overlapping threshold level ranges.
6. The method of claim 1, wherein said desired threshold level ranges include an erased threshold level range.
7. The method of claim 1, wherein the array of memory cells are grouped into *blocks* of cells wherein the *threshold levels of cells within a selected one of the blocks are changed together to a single given threshold level range* prior to applying said appropriate voltage conditions in parallel to the plurality of cells within said one block.

8. The method of claim 7, wherein individual ones of said blocks include a specific number of memory cells and said plurality of memory cells to which said *appropriate voltage conditions are applied in parallel are less than said specific number*, and additionally comprising repeating for another plurality of cells within said one block said applying, determining and terminating operations.
10. The method of any one of claims 1-9, carried out on a single integrated circuit chip.
12. The method of claim 1 wherein the desired ones of said threshold level ranges reached by applying appropriate voltage conditions to the plurality of memory cells correspond to a *chunk of input data being programmed into the memory system*.
13. The method of claim 12, wherein the plurality of cells are determined to have reached the desired threshold level ranges by *comparing the threshold levels of the plurality of cells with the chunk of input data*.
14. The method of claim 13, wherein *the chunk of input data is stored in a cache memory prior to being programmed into memory cells* within the EEprom.

2. Disputed Claim Terms

a. Claim 1 - In General

A major underlying dispute between the parties is whether claim 1 is directed towards a “program operation” only, or whether claim 1 also covers an “erase operation.”¹⁷⁴ SanDisk asserts that claim 1 is only directed to programming. Both ST and Staff assert that claim 1 is not limited to programming and can be directed to erasing as well.

¹⁷⁴ Although the undersigned is not in agreement with ST that SanDisk’s “overview” violates Ground Rule 8.2, which is discussed below, the undersigned does find that the inclusion of this “overview” section by SanDisk has made it difficult to analyze the parties’ specific claim construction arguments. Generally, the undersigned requires parties to follow the same general outline for their briefs in order to be able to easily identify each party’s position on a particular issue. See Ground Rule 11.3. The undersigned does not require a joint narrative statement of issues, as some other ALJs may require, because the undersigned would like to give the parties as much latitude in preparing their briefs as they’d like. If parties cannot, however, agree to which claim terms are actually in dispute, then the undersigned will require parties to prepare an outline before the briefs are due and adhere to it strictly. It is difficult enough to analyze claim construction issues without having to find where the arguments are for a particular disputed issue.

SanDisk asserts that the term “desired threshold level range” corresponds to a “desired” state that results from programming, not erasing.¹⁷⁵ In support, SanDisk points to the specification, which it alleges only refers to states and threshold levels that result from a program operation as “desired,” while it refers to the state that results from an erase operation as the “erased” state.¹⁷⁶

SanDisk also asserts that dependent claim 7 supports its claim construction. According to SanDisk, claim 7 clearly refers to a block erase operation, which is described as a “single given threshold level range.” SanDisk contrasts this term with “desired threshold level ranges” in claim 1. Because of the difference in terminology, “desired” in claim 1 versus “single given” in claim 7, SanDisk asserts that they are referring to two different operations.¹⁷⁷

Furthermore, SanDisk points to the prosecution history which refers to application claim 63 (issued claim 1) as directed to:

[P]rogramming a group of non-volatile memory cells by applying programming conditions to the cells in the group, monitoring their programmed states, and then terminating application of the programming conditions on a cell-by-cell basis as they reach their respective programmed states corresponding to data that is being stored in the memory.¹⁷⁸

SanDisk also argues that the issue of whether “altering” refers to adding or removing a charge is distinct from whether claim 1 only covers a program operation. According to SanDisk, whether or not the undersigned construes “altering” to include adding and removing a charge from the floating gate, this does not necessarily mean that claim 1 also covers an erase operation because of

¹⁷⁵ CIB 6 citing CX-99/RX-2 (the ‘517 patent) at col 21:33-34, 27:22-25, 27:60-64, 28:8-17.

¹⁷⁶ CIB 7-8.

¹⁷⁷ CIB 9-10.

¹⁷⁸ CIB 10 citing CX-103/RX-4 (the ‘517 prosecution history) at SDITC-II-12603//ST560-H 17083-84.

the separate “desired threshold level ranges” limitation.¹⁷⁹ SanDisk, however, concedes that the convention used for programming is to add or remove charge.¹⁸⁰

ST counters all of SanDisk’s arguments. First, ST asserts that SanDisk has waived construing the term “desired” to “programming” because they did not preserve this issue in the pre-hearing brief.¹⁸¹ Second, ST asserts that because claim 1 refers to “appropriate voltage conditions . . . to alter” a cell’s floating gate charge, the claim covers removing a charge.¹⁸² According to ST, even SanDisk’s experts agree that the plain meaning of the claim includes erasing.¹⁸³ Furthermore, ST argues that SanDisk specifically told the Patent Office that claim 1 covered programming and erasing during prosecution.¹⁸⁴

The undersigned addresses the procedural issue first. As for ST’s argument that SanDisk failed to preserve the issue of construing the term “desired,” the undersigned finds that, although SanDisk could have briefed this issue with more specificity in its prehearing brief by clearly labeling it as a disputed claim term, it is hereby determined that it was sufficiently preserved.¹⁸⁵

Now, as to the substantive arguments, the undersigned finds ST and Staff’s arguments to be persuasive. The strongest support for ST and Staff’s position comes from looking at claims 1 and 6. Claim 6, which depends from claim 1, reads as follows:

¹⁷⁹ CIB 11.

¹⁸⁰ CIB 11, n. 6, which states that the usual convention in the industry, as testified by Dr. Subramanian, is to program by adding charge to the floating gate. Subramanian, Tr. 1069.

¹⁸¹ RRB 1 citing Ground Rule 8.2.

¹⁸² RRB 1.

¹⁸³ RRB 1 citing Rhyne, Tr. 1771 (“plain meaning of the word to alter includes increasing and decreasing”); Rao, Tr. 3125 (claim 1 “covers erasure”); RPX-22 (water into cup physical exhibit) (“to alter” includes decreasing).

¹⁸⁴ RRB 1.

¹⁸⁵ See SanDisk’s Prehearing Brief at 115 (“These desired ranges correspond to data that is being programmed into the cells.”).

The method of claim 1, wherein said desired threshold level ranges include an erased threshold level range.¹⁸⁶

Based on claim 6 above, it is clear that the “desired threshold level ranges” referred to in claim 1 can include an erased threshold level range. While the “desired threshold level ranges” referred to in claim 1 does not have to include such an erased threshold level range, as is required by claim 6, it can include an erased threshold level range. Therefore, to construe “desired threshold level ranges” as only referring to programming, and not including erasing, would be incorrect.

The undersigned rejects SanDisk’s arguments regarding the comparison of claims 1 and 7. The fact that claim 7 refers to a “single given threshold level range,” rather than “desired threshold level ranges” does not preclude claim 1 from including an erase operation.

While the specification does make repeated reference to a “desired” state that results from programming, rather than erasing, the claims themselves do not limit the construction of “desired” in referring to a program operation exclusively. Furthermore, the specification does make some reference to “desired” with respect to the erasing.¹⁸⁷

The undersigned agrees with Staff that the prosecution history is, at best, ambiguous. While SanDisk asserts that during the prosecution history, the applicants described application claim 63 (issued claim 1) as directed to “programming,” ST also asserts that the applicant’s preliminary amendment also implied that the new claims were intended to encompass not only those claims of the ‘338 patent that cover programming, but also those claims of the ‘338 patent, *i.e.* claim 40, that

¹⁸⁶ CX-99/RX-2 (the ‘517 patent) at col. 31:9-10.

¹⁸⁷ CX-99/RX-2 (the ‘517 patent) at col. 7:61 (“desired to be erased”) and col. 7:10 (“desired sector” for erasure).

covers erasing.”¹⁸⁸ In the absence of a clear disclaimer of scope, the prosecution history cannot change the meaning of the claims.¹⁸⁹ In this instance, the prosecution history does not help clarify the meaning of the claim term. Therefore, it will not be considered.

Based on the above, the undersigned finds it unnecessary to address the parties’ arguments regarding whether term “alter” necessarily means that claim 1 covers programming and erasing. “Alter” will be construed in further detail below.

Therefore, a reading of the claims themselves supports the undersigned’s finding that the term “desired” is not limited to programming. Accordingly, the undersigned finds that claim 1 is directed toward a “program operation” as well as an “erase operation.”

b. “EEPROM system” (claim 1)

SanDisk asserts that the claim term “EEPROM system” should be construed as “a system that includes one or more EEPROM arrays under the control of a controller.”¹⁹⁰ Staff agrees.¹⁹¹ ST asserts that the term “EEPROM system” is not a limitation of claim 1 and need not be construed because it is a non-limiting introduction to the method steps that follow in the claim.¹⁹²

SanDisk asserts that its construction is based on the plain meaning of the term “EEPROM system” as known by a person of ordinary skill in the art.¹⁹³ Staff asserts that, because the claims cover a method of operation, the device must have some sort of controller in order to operate the

¹⁸⁸ CX-103/RX-4 (the ‘517 prosecution history) at SDITC-II 12567/ST560-H 17074; Rhyne, Tr. 1785-86.

¹⁸⁹ *Markman*, 52 F.3d at 980.

¹⁹⁰ CIB 14 citing CX-2229C (Rhyne Direct) at Q. 415.

¹⁹¹ SIB 28 citing CX-99/RX-2 (“the ‘517 patent”) at col. 2:1-3; 4:32-33; 5:1-3; 7:22-24; 20:22-26.

¹⁹² RIB 3.

¹⁹³ See, *infra*, Section V(D)(1).

device.¹⁹⁴

The undersigned finds SanDisk and Staff's arguments persuasive and that the term "EEPROM system" should be construed. As SanDisk and Staff are the only parties that proposed a claim construction for this claim term, their claim construction is hereby adopted, which is construed consistently with the specification.¹⁹⁵ Accordingly, the phrase "EEPROM system" in claim 1 is construed to mean: **"a system that includes one or more EEPROM arrays under the control of a controller."**

c. "Electrically floating gate" (claim 1)

SanDisk asserts that the claim term "electrically floating gate" should be construed as "a gate that is surrounded by a dielectric material so as to be insulated from other conductive elements."¹⁹⁶ ST does not propose a construction for this claim term. Staff asserts that, because there is no substantive dispute over this claim limitation, it does not need to be construed.¹⁹⁷ As there is no real dispute, the claim construction proposed by SanDisk is hereby adopted, which is supported by the specification.¹⁹⁸

Accordingly, the phrase "electrically floating gate" in claim 1 is construed to mean: **"a gate that is surrounded by a dielectric material so as to be insulated from other conductive elements."**

¹⁹⁴ SIB 28.

¹⁹⁵ CX-99/RX-2 ("the '517 patent") at col. 2:1-3 ("A Flash EEPROM memory system comprises one or more Flash EEPROM chips under the control of a controller.").

¹⁹⁶ CIB 14 citing CX-2229C (Rhyne Direct) at Q. 417.

¹⁹⁷ SIB 13.

¹⁹⁸ CX-99/RX-2 ("the '517 patent") at col. 18:39-44 ("Each of the memory cells 1011 and 1013 contains respective conductive floating gates 1023 and 1025, generally made of polysilicon material. Each of these floating gates is surrounded by dielectric material so as to be insulated from each other and any other conductive elements of the structure.").

d. “Alterable” (claim 1)

SanDisk does not give a straightforward claim construction for this claim term. Instead, SanDisk argues that both ST and Staff are confusing the two distinct issues of whether “altering the charge” on the floating gate is limited to adding charge to the floating gate, or can also mean removing a charge, and whether claim 1 covers only a program operation or also covers an erase operation.¹⁹⁹ According to Staff, while SanDisk argued that “alterable” should be construed as “increasing the charge level,” *i.e.*, programming the cell, in its pre-hearing brief,²⁰⁰ SanDisk has now reversed course and appears to concede that “alterable” refers to both adding and subtracting charge.²⁰¹ ST asserts that the term “alterable” should be construed as “increasing the charge levels or decreasing the charge levels.”²⁰² Staff agrees with ST.²⁰³

ST asserts that the plain meaning of “to alter the charge levels” undisputedly includes increasing the charge levels or decreasing the charge levels.²⁰⁴ According to ST, the specification expressly discloses altering the charge levels by applying appropriate voltage conditions to decrease them, which is consistent with the plain meaning of the term.²⁰⁵ ST asserts that SanDisk’s claim construction, limiting claim 1 to programming, should be rejected because it is contrary to the plain meaning of the term.²⁰⁶

¹⁹⁹ CIB 10-11.

²⁰⁰ Complainants’ Prehearing Brief 120-29.

²⁰¹ SRB 12 citing CIB 11.

²⁰² RIB 5-6.

²⁰³ SIB 29.

²⁰⁴ RIB 5 citing RX-1801C (Subramanian Direct) at 81-83; RX-2153C (Subramanian Rebuttal) at 33-39; Rhyne, Tr. 1771.

²⁰⁵ RIB 5-6 citing RX-1801C (Subramanian Direct) at 83-85; RX-2153C (Subramanian Rebuttal) at 39-44; Rhyne, Tr. 2369-74; RDX-40.

²⁰⁶ RIB 6 citing RX-1801C (Subramanian Direct) at 85-87; RX-2153C (Subramanian (continued...))

Staff asserts that the plain meaning of “alter” is “to change.”²⁰⁷ In addition, Staff notes that when a claim in the ‘517 patent is limited to programming, the term “programming” is used, rather than the term “alter.” And when different words or phrases are used in separate claims, a difference in meaning is presumed.²⁰⁸

All parties agree that the conventional use of the term “alter” refers to both increasing and decreasing.²⁰⁹ The undersigned finds that there is no indication in the specification that the applicant chose to assign a different meaning to “alterable” than its plain meaning.

Accordingly, the phrase “alterable/to alter” in claim 1 is construed to mean: **“increasing or decreasing.”**

e. “Appropriate voltage conditions” (claim 1)

SanDisk asserts that the claim term “appropriate voltage conditions being applied to the cell in order to set a variable threshold level thereof into a range that is determinable by reading the cell” should be construed as referring to “one or more program voltage pulses that individually shift the threshold level of the cell into a threshold level range corresponding to a state.”²¹⁰ ST does not propose a claim construction for this claim term in its brief.²¹¹ Staff asserts that “appropriate voltage conditions” should not be restricted to any particular types of voltage conditions, but should include all voltage conditions that one of ordinary skill in the art would understand were appropriate to alter

²⁰⁶(...continued)

Rebuttal) at 44-47; Rhyne, Tr. 1786.

²⁰⁷ SIB 29 citing WEBSTER’S THIRD NEW INTERNATIONAL DICTIONARY 63 (1981).

²⁰⁸ SIB 29 citing *Nystrom v. TREX Co.*, 424 F.3d 1136, 1143 (Fed. Cir. 2005) (“*Nystrom*”).

²⁰⁹ SanDisk’s expert, Dr. Rhyne, conceded at trial that “to alter includes increasing and decreasing” (Rhyne, Tr. 1771); RIB 5; SIB 29-31.

²¹⁰ CIB 14 citing CX-2229C (Rhyne Direct) at Q. 418.

²¹¹ Staff notes, however, that ST has addressed this issue in their findings of fact. SRB 12.

the charge level of the floating gate.²¹² In other words, SanDisk asserts that the claim only covers hot electron injection, while Staff asserts that the claim covers both hot electron injection and Fowler-Nordheim tunneling.²¹³

SanDisk asserts that the plurality of cells to which the “appropriate voltage conditions” are applied reach their “desired threshold level ranges.” SanDisk argues that cells reach their “desired threshold level ranges” as the result of a program operation, not an erase operation. Therefore, according to SanDisk, “appropriate voltage conditions” are conditions for programming, not erasing. SanDisk asserts that its claim construction is correct based on claim differentiation and points to dependent claim 7. According to SanDisk, the block erase operation in claim 7 occurs “prior to applying said appropriate voltage conditions in parallel” to a plurality of cells within the block. SanDisk argues that claim 7’s reference back to the “said appropriate voltage conditions,” which is recited in claim 1 necessarily means that “said appropriate voltage conditions” are those required to perform a program operation, not an erase operation.²¹⁴

Staff asserts that both SanDisk’s and ST’s experts agree that, although the ‘517 patent only discloses programming by means of hot electron injection, one of ordinary skill in the art would understand that Fowler-Nordheim tunneling could also be used to program cells.²¹⁵ Staff also asserts that the specification discloses the use of hot electron injection for programming and Fowler-Nordheim tunneling for erase.²¹⁶ In addition, the Staff notes that the specification refers to voltage conditions that both the ‘517 and ‘338 patents list for erase are those conditions used to create

²¹² SIB 31.

²¹³ SIB 31.

²¹⁴ CIB 14 citing CX-2229C (Rhyne Direct) at Q. 418.

²¹⁵ SIB 31 citing CX-2229C (Rhyne Direct) at 331; Subramanian, Tr. 1227-28.

²¹⁶ SRB citing Rhyne, Tr. 1828; Subramanian, Tr. 1083-85.

Fowler-Nordheim tunneling.²¹⁷

As noted above, the undersigned rejected SanDisk's argument that claim 1 is solely directed to programming. As SanDisk has not presented any other arguments, SanDisk's claim construction is rejected. In addition, the undersigned finds Staff's arguments persuasive. The Federal Circuit has "expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment."²¹⁸

Accordingly, the phrase **"appropriate voltage conditions"** in claim 1 is construed to mean: **"all voltage conditions that are appropriate to alter the charge level of the floating gate."** In other words, claim 1 covers both hot electron injection and Fowler-Nordheim tunneling.

f. "Applying said appropriate voltage conditions in parallel to a plurality of said memory cells" (claims 1 and 7)

SanDisk asserts that the claim term "applying said appropriate voltage conditions in parallel to a plurality of said memory cells" should be construed consistently as the term was construed above. In addition, SanDisk asserts that the phrase "in parallel to a plurality of memory cells" should be construed as "two or more cells receive the recited appropriate voltage conditions simultaneously," which SanDisk asserts is not in dispute.²¹⁹ ST asserts that the "plurality" is limited solely to cells whose threshold level ranges are intentionally changed by performing the claimed applying appropriate voltage conditions step.²²⁰ Staff asserts that the claim term should be construed

²¹⁷ SIB 31 citing Subramanian, Tr. 1083-85; CX-98/RX-1 (the '338 patent), figs. 18-19; CX-99/RX-2 (the '517 patent), figs. 26-27.

²¹⁸ *Phillips*, 415 F.3d at 1323.

²¹⁹ CIB 14-15.

²²⁰ RIB 3-4 citing RDX-57.

to mean that “appropriate voltage conditions are applied to two or more cells simultaneously.”²²¹

Staff asserts that the dispute between the parties is what is meant by “said” appropriate voltage conditions. According to Staff, ST asserts that the same voltage conditions must always be applied in the same operation. In other words, once the device applies a particular set of voltage conditions to alter the charge level, it must continue exactly the same voltage conditions, *i.e.* the device must apply constant voltage pulses.²²² Staff asserts that, because the preamble refers to voltage conditions appropriate to alter the charge level of the floating gate in order to set a threshold level for the cell, the “said appropriate voltage conditions” are the same voltage conditions. Therefore, the “said appropriate voltage conditions” should not be limited to constant or increasing pulses.²²³

The undersigned finds Staff’s arguments to be persuasive. The use of the term “said” in a patent specifically refers to an antecedent basis.²²⁴ The term “said” does not change the meaning of the antecedent to which it refers.²²⁵ As the undersigned has already construed the term “appropriate voltage conditions” above, the reference to “said appropriate voltage conditions” is construed the same. In addition, the parties appear to agree on the meaning of the term “plurality” as “two or more.”²²⁶

Accordingly, the phrase “**applying said appropriate voltage conditions in parallel to a plurality of said memory cells**” in claims 1 and 7 is construed to mean: “**appropriate voltage**

²²¹ SIB 32 citing CX-99/RX-2 (the ‘517 patent) at col. 21:31-47, 27:20-45; Fig. 23.

²²² SIB 33 citing Respondents’ prehearing brief 63-70.

²²³ SIB 33; SRB 14-15.

²²⁴ MPEP § 2173.05(e) (8th ed. 2005); *Energizer Holdings, Inc. v. Int’l Trade Comm’n*, 435 F.3d 1366, 1370 (Fed. Cir. 2006) (“*Energizer*”).

²²⁵ See *In re Self*, 671 F.2d 1344, 1347 (C.C.P.A. 1982) (“*Self*”).

²²⁶ CIB 15, RIB 3, SIB 32.

conditions are applied to two or more cells simultaneously.”

g. “Determining the threshold level ranges in which individual ones of said plurality of memory cells lie” (claim 1)

SanDisk asserts that the claim term “determining the threshold level ranges in which individual ones of said plurality of memory cells lie” should be construed as “determining, on a cell-by-cell basis, in which threshold level range an individual cell undergoing programming lies.”²²⁷ ST asserts that the term should be construed as “requiring, for each memory cell in the plurality, establishing the threshold level range in which its inversion layer forms.”²²⁸ Staff asserts that the claim term should be construed as “referring to determining the threshold level range in which each cell of the plurality lies.”²²⁹

SanDisk asserts that its claim construction is supported by the specification. Pointing to Figures 14 and 15A, SanDisk asserts that the specific threshold level range for a particular cell defines the state of that cell. Therefore, there is a one-to-one correspondence between a cell’s state and the threshold level range in which the cell lies. SanDisk also asserts that the specification explains that the state of cell may be defined in terms of either threshold level ranges or the source-drain current ranges that correspond to the threshold level ranges.²³⁰ According to SanDisk, the corresponding source-drain current window for Figure 15A is shown in Figure 15B. Therefore, SanDisk asserts that the specification treats threshold voltage and source-drain current as interchangeable and that either voltage or source-drain current can be used to determine the cell’s

²²⁷ CIB 15.

²²⁸ RIB 6 citing RDX-59.

²²⁹ SIB 33-34 citing CX-99/RX-2 (the ‘517 patent) at Figs. 14A, 15B; col. 21:15-30, 21:48-55, 22:43-23:60.

²³⁰ CIB 16 citing CX-2229C (Rhyne Direct) at Q. 450.

state and threshold level range.²³¹

SanDisk also asserts that the “determining” step includes, but does not require “margining.” According to SanDisk, “margining” is used during the verify read operation to ensure that minor variations do not impact the one-to-one correspondence between a programmed cell’s threshold level range and its state. SanDisk asserts that, because claim 16 depends from claim 1, and adds the limitation that programming of cells is terminated “upon their being determined to have been programmed to within the desired threshold levels by a margin,” the determining step provides a margin to ensure that, when the cell is programmed, there is a one-to-one correspondence between the cell’s threshold level range and its state.²³²

Staff asserts that the dispute over this limitation appears to be whether this method step requires measuring the threshold level of each cell, or whether any method of determining the range into which the cell falls may be used. According to Staff, while Figure 15A compares threshold levels directly, Figure 15B compares threshold levels indirectly by measuring the source-drain current. Staff asserts that the “determining” step in claim 1 requires determining the memory state of the cell in relation to a threshold level range, but that it does not require the measuring of the threshold level of cells to be direct.²³³ Therefore, Staff states that this claim limitation is not limited to measuring the threshold voltage directly, but it is limited to cases in which the memory state of

²³¹ CIB 16.

²³² CIB 17 citing CX-99/RX-2 (the ‘517 patent) at col. 30:14-19, 31:58-62.

²³³ SIB 34 citing CX-99/RX-2 (the ‘517 patent) at figs. 15A-15B, col. 22:60-66 (“Just as the breakpoint threshold levels (*see* FIGS. 14 and 15A) are used to demarcate the different regions in the threshold voltage window, the I_{REF} levels are used to do the same in the corresponding source-drain current window. By comparing with the I_{REF} ’S, the conduction state of the memory cell can be determined.”)

the cell is determined by reference to its threshold voltage.²³⁴

ST opposes both SanDisk and Staff. According to ST, claim 1 does not recite determining a “state,” it recites determining a “threshold level range,” which is not the same thing.²³⁵ ST asserts that “state” is a much broader term than “threshold level range,” and that SanDisk’s attempt to use such a broad generic term be rejected.²³⁶ ST asserts that SanDisk’s expert, Dr. Rhyne, conceded that the “threshold level of a memory cell is a cell’s threshold voltage” which is the control gate voltage at which an inversion layer forms in the cell’s channel region allowing source drain conduction to begin.²³⁷ ST argues that, while there can be a relationship between conduction and threshold voltage, conduction is not the same thing as threshold voltage.²³⁸ ST asserts that a comparison of Figures 15A and 15B supports its argument, as the specification describes these alternative metrics. According to ST, these two figures depict two cells that have different conduction states, but are conceded to have the identical threshold level range, *i.e.* both in range 1353.²³⁹ ST argues that, because SanDisk recited “threshold level range” in this claim term, that the “threshold voltage” metric is the one that must be used to assign states, not conduction.²⁴⁰ ST asserts that, by the patent’s own disclosure, claim 1 does not encompass every technique capable of assigning states to cells.²⁴¹

The undersigned does not adopt SanDisk’s claim construction’s reference limiting the claim

²³⁴ SRB 15.

²³⁵ RIB 6.

²³⁶ RIB 8.

²³⁷ RIB 6 citing Rhyne, Tr. 1881-82. *See also* RX-1801C (Subramanian Direct) at 94-102; RX-2153C (Subramanian Rebuttal) at 57-66; JX-39C (Norman Dep) at 179-80.

²³⁸ RIB 7 citing Rhyne, Tr. 1884, 1910.

²³⁹ RRB 6 citing Rhyne, Tr. 1910; RX-2153C (Subramanian Rebuttal) at 450-53.

²⁴⁰ RRB 6-7 citing RX-1801C (Subramanian Direct) at A. 355-72; RX-2153C (Subramanian Rebuttal) at A. 453, 459-61.

²⁴¹ RRB 7 citing *Unique Concepts, Inc. v. Brown*, 939 F.2d 1558, 1562-63 (Fed. Cir. 1991) (“*Unique Concepts*”).

to “programming,” which was rejected above. The undersigned also does not adopt SanDisk’s “margin” argument because there is no evidence that the applicant intended to encompass margin as part of the “determining” claim limitation. While there is a reference to margin in the specification, care should be taken not to import a limitation into the claim from the specification.²⁴²

The undersigned also does not find ST’s arguments to be persuasive. There is no mention of “inversion layers” anywhere in the specification; therefore ST’s claim construction will not be adopted. In addition, while the undersigned agrees that conduction is not the same thing as threshold voltage, there is a relationship between the two so that one can determine threshold voltage from conduction.

The undersigned finds Staff’s arguments to be persuasive. Based on the claim language, measuring the threshold level of each cell is not required as long as a method is used to determine the range into which the cells falls. The specification describes two figures which compare threshold level—Figure 15A compares it directly, while Figure 15B compares it indirectly by measuring the source-drain current:

Just as the breakpoint threshold levels (see FIGS. 14 and 15A) are used to demarcate the different regions in the threshold voltage window, the I_{REF} levels are used to do the same in the corresponding source-drain current window. By comparing with the I_{REF} ’s, the conduction state of the memory cell can be determined.²⁴³

Therefore, the claim limitation is met when the memory state of the cell is determined by reference to its threshold voltage, whether that be directly or indirectly.

Accordingly, the phrase “**determining the threshold level ranges in which individual ones**

²⁴² *Bell Atlantic*, 262 F.3d at 1270.

²⁴³ CX-99/RX-2 (the ‘517 patent) at figs. 15A-15B, col. 22:60-66.

of said plurality of memory cells lie” in claim 1 is construed to mean: “referring to determining the threshold level range in which each cell of the plurality lies.”

h. “Terminating said application of appropriate voltage conditions to individual ones of said plurality of memory cells” (claim 1)

SanDisk asserts that the claim term “terminating said application of appropriate voltage conditions to individual ones of said plurality of memory cells” should be construed as meaning that “an individual cell that has been determined to fall within its desired threshold level range will not receive additional applications of appropriate voltage conditions for the remainder of the program operation, and the program operation ends.”²⁴⁴ ST asserts that the term should be construed as “when a cell is first determined to have reached its desired threshold level range, preventing all further alteration of the charge level on the memory cell’s floating gate.”²⁴⁵ Staff asserts that the claim term should be construed to mean that “an individual cell that has been determined to fall within its desired threshold level range will not receive additional applications of appropriate voltage conditions for the remainder of the program operation.”²⁴⁶

SanDisk asserts that its claim construction is consistent with the plain meaning of the term “terminating” and that it is consistent with the description in the specification and prosecution history.²⁴⁷ For example, when a cell is verified as having reached its desired threshold level range,

²⁴⁴ CIB 17.

²⁴⁵ RIB 8 citing RDX-60.

²⁴⁶ SIB 34-35 citing CX-99/RX-2 (the ‘517 patent) at Fig. 23(6); col. 3:62-4:13, 21:35-42, 27:22-30, 28:8-17, 29:5-10, 29:60-64.

²⁴⁷ CIB 18 citing CX-2229C (Rhyne Direct) at Q. 479, 481; CX-2298C (Rhyne Rebuttal) at Q.48-49; CX-103/RX-4 (the ‘517 prosecution history) at SDITC-II-17083-84/SDITC-II-012603-04, 12567; CX-102/RX-5 (“the ‘338 reexamination”) at SDITC-II-14444-46, 14636/SDITC-II-0001983-85.

its programming terminates.²⁴⁸

Staff agrees with SanDisk. Staff asserts that the main dispute over the construction of this claim limitation is whether the claim prohibits “program disturb,” in other words, whether terminating the application of appropriate voltage conditions means terminating the transfer of any electrons to the floating gate. Staff argues that the plain meaning of the term requires terminating the application of appropriate voltage conditions to a cell when that cell reaches the correct threshold level range. According to Staff, the fact that there is incidental leakage of charge because appropriate voltage conditions continue to be applied to other cells is irrelevant.²⁴⁹

ST asserts that its claim construction is supported by the prosecution history because the applicants made a clear and unmistakable disclaimer as to what “terminating” means in order to distinguish the ‘517 patent from the prior art.²⁵⁰ According to ST, SanDisk told the examiner that latch 1721 is set when a cell reaches its desired threshold level range, and “[s]etting of this latch terminates any further alteration of the charge of its associated cell that might result from further application of the appropriate voltage conditions to others of the plurality of cells being programmed in parallel.”²⁵¹ ST argues that Dr. Rhyne agreed that latch 1721 is the only enabling disclosure of cell-by-cell inhibiting.²⁵²

ST also asserts that its claim construction is supported by the claim construction in the 526

²⁴⁸ CIB 18 citing CX-2229C (Rhyne Direct) at Q. 475-78; CX-99/RX-2 (the ‘517 patent) at col. 3:62-4:1, 21:35-42, 27:18-26, 62-64, 28:8-17, 29:4-9, 60-62 Fig. 23; CX-2226C (Mehrotra Direct) at Q. 178-80, 184, 188, 192, 196, 202, 207.

²⁴⁹ SIB 35.

²⁵⁰ RIB 8.

²⁵¹ RIB 8 citing CX-103/RX-4 (the ‘517 prosecution history) at SDITC-II 12646/ST560-H 17181.

²⁵² RIB 9, RRB 7 citing Rhyne, Tr. 2029-30.

investigation. According to ST, Judge Luckern adopted SanDisk's construction of the "means for inhibiting" limitation, where SanDisk represented to Judge Luckern that a memory cell will not have any additional electrons added to its floating gate once terminating occurs.²⁵³ According to ST, SanDisk concedes that its current position is inconsistent with the representations made to Judge Luckern.²⁵⁴

SanDisk counters ST arguments. According to SanDisk, ST's claim construction rewrites the plain language of the claim, is unsupported by the description in the specification, and is unsupported by the prosecution history.²⁵⁵

Staff also counters ST's arguments. According to Staff, ST's reference to the prosecution history does not relate to claim 1 of the '517 patent, but refers to claim 37 of the patent which requires preventing the application of appropriate voltage conditions to other cells in the plurality from altering the charge level of the inhibited cell.²⁵⁶

The undersigned finds SanDisk and Staff's arguments to be persuasive because their claim construction most closely resembles the plain and ordinary meaning of the term "terminating." In addition, ST's reference to the prosecution history does not support ST's arguments, as the cited reference does not even relate to application claim 63 (issued claim 1). Rather, the statement refers to application claim 100 (issued claim 37), which does not include any "terminating" language and is not at issue in this investigation. In order for there to be a disclaimer, it must be clear in the

²⁵³ RIB 9 citing Rhyne, Tr. 2033-35; CX-372C (the 526 ID) at 49-50.

²⁵⁴ RIB 9 citing Rhyne, Tr. 2035.

²⁵⁵ CIB 18 citing CX-2229C (Rhyne Direct) at Q. 483, 485, 487-89; Subramanian, Tr. 1210-11; CX-99/RX-2 (the '517 patent) at col. 21:42-47.

²⁵⁶ SIB 35 citing CX-103/RX-4 (the '517 prosecution history) at SDITC-II 12646/ST560-H 17181; SRB 15-16.

prosecution history.²⁵⁷ In this instance, the undersigned does not find that such a disclaimer was made. As to ST's argument that SanDisk's current position is inconsistent with the representations made to Judge Luckern during the 526 investigation, the undersigned finds that such argument is not convincing because the disputed claim term in the 526 investigation was the "means for inhibiting further programming of correctly verified cells among the plurality of addressed cells," which is different than this disputed claim term.²⁵⁸

Accordingly, the phrase **"terminating said application of appropriate voltage conditions to individual ones of said plurality of memory cells"** in claim 1 is construed to mean: **"an individual cell that has been determined to fall within its desired threshold level range will not receive additional applications of appropriate voltage conditions for the remainder of the program operation."**

i. **"Continuing to apply said appropriate voltage conditions to others of said plurality of cells" (claim 1)**

SanDisk asserts that the claim term "continuing to apply said appropriate voltage conditions to others of said plurality of cells" should be construed as consistent as the term "appropriate voltage condition" was construed above.²⁵⁹ Staff agrees that this claim term should be construed consistently with how "appropriate voltage conditions" was construed above.²⁶⁰ ST asserts that the term should be construed as "continuing to apply the same set of voltage conditions as used at the outset of the

²⁵⁷ See *Markman*, 52 F.3d at 980 (in the absence of a clear disclaimer of scope, the prosecution history cannot change the meaning of the claims); *Superguide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) ("*Superguide*").

²⁵⁸ CX-372C (the 526 ID) at 47.

²⁵⁹ CIB 18.

²⁶⁰ SRB 14.

operation.”²⁶¹

SanDisk asserts that the appropriate voltage conditions are not limited to a single set of voltage conditions, which is reflected by the use of the term “voltage conditions,” which is plural. According to SanDisk, in 1989 it was well-known that a wide range of program pulse techniques could be used to apply “appropriate voltage conditions” to a cell, including ramped programming pulses as well as constant programming pulses.²⁶²

Staff asserts that the use of the word “continuing” does not mean that the same specific voltages must always be applied because the claim covers “continuing to apply said appropriate voltage conditions,” which Staff construed above as voltage conditions appropriate to alter the charge level.²⁶³ While Staff acknowledges that the claim term excludes voltage conditions appropriate for reading, the claim does include voltage conditions that program or erase the cell, such as both constant voltage pulses and incremental step pulse programming.²⁶⁴

ST asserts that the claim term “continuing to apply said appropriate voltage conditions” should refer to the same set of voltage conditions that were used in the first “applying” step.²⁶⁵ ST argues that the use of the term “continuing to apply said” refers back to the “applying” step; therefore, the “continuing” step requires the same exact voltage conditions as in the “applying”

²⁶¹ RIB 10 citing RDX-61.

²⁶² CIB 18 citing CX-2229C (Rhyne Direct) at Q. 419-20, 429; Pashley, Tr. 2763-65; CX-2225C (Harari Direct) at Q. 108; RX-1801C (Subramanian Direct) at Q. 258; CX-110 (the ‘685 patent) at Abstract.

²⁶³ SRB 14-15.

²⁶⁴ SRB 14.

²⁶⁵ RRB 5 citing *Phillips*, 415 F.3d at 1316.

step.²⁶⁶ ST asserts that the specification and prosecution history support its position.²⁶⁷

The undersigned agrees with SanDisk and Staff that “continuing to apply said appropriate voltage conditions” should be construed consistently with “appropriate voltage conditions” and “said appropriate voltage conditions” above. The claim construction does not require the same exact voltage conditions. While the use of the term “continuing” may imply that the only one set of voltage conditions needs to be applied, it was determined above that there are multiple conditions that may be applied in order to alter the charge level of the floating gate in order to set a threshold level for the cell.

Accordingly, the phrase **“continuing to apply said appropriate voltage conditions to others of said plurality of cells”** in claim 1 is not limited to the same set of voltage conditions as used at the outset of the operation and refers to **“all voltage conditions that are appropriate to alter the charge level of the floating gate.”**

j. **“Until all of the plurality of cells are determined to have reached their desired threshold level ranges” (claim 1)**

SanDisk asserts that the claim term “until all of the plurality of cells are determined to have reached their desired threshold level ranges” should be construed as “meaning that the recited programming steps will be performed until all of the plurality of cells are determined to have reached their desired threshold level ranges, at which point the EEPROM system stops the program operation.”²⁶⁸ ST asserts that the term should be construed as “once the threshold level of each cell in the plurality has been established to have moved into the desired one of the two or more potential

²⁶⁶ RIB 10-11 citing Rhyne, Tr. 1830; RX-1801C (Subramanian Direct) at 77-78, 126-27.

²⁶⁷ RIB 11 citing Rhyne, Tr. 1832-40; RX-1801C (Subramanian Direct) at 78-79, 255; CX-103/RX-4 (the ‘517 prosecution history) at SDITC-II 12603/ST560-H 17083.

²⁶⁸ CIB 19.

ending ranges, the terminating, determining and applying steps stop.”²⁶⁹ Staff asserts that the claim term should be construed to mean that “the application of appropriate voltage conditions to cells in the plurality will continue until all cells in the plurality have reached the desired threshold level ranges, at which point application of the appropriate voltage conditions stops.”²⁷⁰

SanDisk asserts that the plain meaning of “until” requires the system to affirmatively determine that all of the plurality of cells have reached their desired threshold level ranges. According to SanDisk, the determination is what causes the application of further appropriate voltage conditions to stop. SanDisk points to the specification in support.²⁷¹

ST asserts that claim 1 requires the steps of “applying,” “determining,” “terminating,” and “continuing to apply” to continue until all of the plurality of cells are determined to have reached their desired threshold level ranges. ST argues that the claim is explicit in that only “the plurality” are relevant to the “ranges” requirement. Therefore, according to ST, what claim 1 requires is that the plurality include some cells whose threshold levels reach one ending range and other cells whose threshold levels reach a second, different ending range.²⁷²

Staff opposes both SanDisk’s and ST’s argument. Staff opposes SanDisk’s arguments because SanDisk asserts that claim 1 only covers programming because cells being erased have only a single desired threshold level range, the erased state. Staff opposes ST’s arguments because ST asserts that claim 1 only covers multi-level cells because the cells whose charge levels are being

²⁶⁹ RIB 3 citing RDX-62.

²⁷⁰ SIB 35-36 citing CX-99/RX-2 (the ‘517 patent) at Fig. 23(5)-(7); col. 28:66-29:10, 29:29-41.

²⁷¹ CIB 19 citing CX-2229C (Rhyne Direct) at Q. 499-503; CX-99/RX-2 (the ‘517 patent) at col. 28:8-20, 29:29-34, Figs. 13, 24; Pashley, Tr. 2558.

²⁷² RIB 4 citing RX-1801C (Subramanian Direct) at 128-31; RX-2153C (Subramanian Rebuttal) at 104-08; Rhyne, Tr. 1764.

altered must reach more than one desired threshold level range. Staff asserts that its claim construction is exactly what is disclosed in the specification, where both single-level and multi-level cells, and both programming and erase, are described.²⁷³ Staff also asserts that, because dependent claims 2 and 4 cover single level cells, and dependent claims 3 and 5 cover multilevel cells, independent claim 1 must cover both. In addition, Staff asserts that dependent claim 10 requires that the claimed method be carried out on a single chip, which implies that the methods of claims 2 and 4 can be performed on a single chip.²⁷⁴

The undersigned does not adopt SanDisk's claim construction because it incorporates a "programming" requirement that was rejected above. The undersigned also does not adopt ST's claim construction because the use of the term "ranges" does not necessarily require that there be more than one desired threshold level range for the plurality of cells because such construction would make claim 1 inconsistent with certain dependent claims, such as claim 10 which covers the use of a single chip with single level cells.²⁷⁵

The undersigned finds Staff's arguments persuasive. The fact that the plurality of addressed cells must reach their desired ranges does not mean that each cell must have more than one desired threshold level range. Rather, it means that each cell must reach its range and the cells together must reach their ranges.²⁷⁶ In addition, the scope of an independent claim must encompass the scope of a claim that depends from it.

Accordingly, the phrase **"until all of the plurality of cells are determined to have reached**

²⁷³ SIB 36 citing CX-99/RX-2 (the '517 patent) at figs. 14, 15A, col. 21:15-60, col. 3:62-4:13.

²⁷⁴ SIB 36.

²⁷⁵ CX-99/RX-2 (the '517 patent) at col. 30:64-65, 31:1-4, 29-30.

²⁷⁶ CX-99/RX-2 (the '517 patent) at figs. 14, 15A, col. 21:15-60, col. 3:62-4:13.

their desired threshold level ranges” in claim 1 is construed to mean: “the application of appropriate voltage conditions ceases when all cells in the plurality are in the desired memory state.” In addition, the claim is not limited to types of cells, such as single-level or multi-level, or operations, such as programming or erasing.

k. “Breakpoint threshold level” (claim 5)

SanDisk asserts that the claim term “breakpoint threshold level” should be construed as “the threshold level that separates one threshold level range from another threshold level range.”²⁷⁷ ST asserts that the term should be construed as “a threshold level that partitions the threshold voltage window or memory cells.”²⁷⁸ Staff asserts that the claim term should be construed to mean “the threshold level that separates one threshold voltage range from another threshold voltage range.”²⁷⁹

While SanDisk and Staff’s constructions are quite similar, the undersigned finds SanDisk’s claim construction most closely reflects the plain meaning of this disputed claim term because of Staff’s extraneous reference to the term “voltage.” Accordingly, the phrase “breakpoint threshold level” in claim 5 is construed to mean: “the threshold level that separates one threshold level range from another threshold level range.”

l. “Blocks” (claims 7 and 8)

SanDisk asserts that the claim term “blocks” should be construed as “the Flash unit of erase, which is substantially larger than a byte or a word.”²⁸⁰ ST asserts that the term should be construed

²⁷⁷ CIB 19-20 citing CX-2229C (Rhyne Direct) at Q. 505-06; CX-99/RX-2 (the ‘517 patent) at col. 21:20-30, 51-53, Fig. 14-15; Subramanian, Tr. 1076-78.

²⁷⁸ RRB 7 citing RX-1801C (Subramanian Direct) at A. 342-54, 416-24; RX-2153C (Subramanian Rebuttal) at A. 421-22, 473, 524.

²⁷⁹ SIB 37 citing CX-99/RX-2 (the ‘517 patent) at Figs. 14, 15A; col. 21:26-28, 21:48-51.

²⁸⁰ CIB 20.

as “some number of cells greater than one that are grouped together for operational purposes.”²⁸¹ Staff asserts that the claim term “blocks of cells” should be construed to mean “groups of multiple memory cells.”²⁸²

SanDisk asserts that its claim construction is consistent with the plain meaning of the term. SanDisk points to the testimony of ST’s expert, Dr. Pashley, who stated that a flash EEPROM “can quickly erase a large block of memory at one time, or in a ‘flash’.”²⁸³ SanDisk also points to the specification which states that a large group of cells that is erased simultaneously is a “block” or “sector” while a smaller group of cells that is programmed simultaneously is a “chunk.”²⁸⁴ Based on its claim construction, SanDisk asserts that claim 7 covers a Flash EEPROM with block erase and the step of performing a block erase occurs prior to programming a plurality of cells within the block; that claim 8 adds a requirement that the plurality of cells programmed is less than the size of a block and that two such pluralities of cells are programmed; and that claim 11 covers performing a block erase on two or more selected blocks.²⁸⁵

Staff asserts that the main dispute regarding this claim term appears to be whether it should be construed as a “unit of erase” and whether the number of cells in the block is substantially larger than a byte or word. Staff notes that the specification uses the term “block” and “sector” interchangeably.²⁸⁶ Staff also points out that the specification states that

In the Flash EEprom array 1060 (FIG. 12), each group of memory cells which is

²⁸¹ RIB 12 citing RDX-64.

²⁸² SIB 37.

²⁸³ CIB 20 citing RX-1802C (Pashley Direct) at Q. 74.

²⁸⁴ CIB 20 citing CX-2229C (Rhyne Direct) at Q. 509-10; CX-99/RX-2 (the ‘517 patent) at col. 7:6-9, 14-17, 14:38-42, 16:4-9, 21:31-33, 25:7-11, 28:7-11, 24-25, 28-30, 38-57.

²⁸⁵ CIB 20.

²⁸⁶ SIB 37 citing CX-99/RX-2 (the ‘517 patent) at col. 7:6-8, 10:45-47.

collectively erased or programmed is called a sector.²⁸⁷

Therefore, Staff asserts that a block is not simply a unit of erase. In addition, Staff points out that the specification does not describe the size of a block. Rather, Staff asserts the specification notes that a sector may have 512 bytes.²⁸⁸

ST agrees with Staff and asserts that a “block” is simply a “groups of cells” that is not limited to a unit of erase.²⁸⁹ ST also points to the same portion of specification noted by Staff above.²⁹⁰ ST also notes that the specification does not limit the size of a block and that the claimed blocks are simply some number of cells greater than one grouped together for operational purposes. Because the term blocks is plural, ST asserts that at least two such blocks are required.²⁹¹

The undersigned finds ST’s and Staff’s arguments to be persuasive because the specification clearly states that a block/sector/group of memory cells, is not simply a unit of erase.²⁹² Although ST agrees that a block is a group of cells, ST proposes a claim construction with additional limitations, such as an “operational purpose,” that is extraneous to what is required to construe the claim. Therefore, the undersigned finds Staff’s claim construction to most clearly reflect the plain meaning of the term.

Accordingly, the phrase “**blocks of cells**” in claims 7, 8, and 11 is construed to mean: “**a group of more than one memory cell.**”

²⁸⁷ SIB 37-38 citing CX-99/RX-2 (the ‘517 patent) at col. 25:7-11.

²⁸⁸ SIB 38 citing CX-99/RX-2 (the ‘517 patent) at col. 7:28-30, 28:28-30.

²⁸⁹ RRB 7-8.

²⁹⁰ RRB 8 citing CX-99/RX-2 (the ‘517 patent) at col. 25:7-11.

²⁹¹ RRB 8 citing RX-1801C (Subramanian Direct) at A. 264-67, 443-49; RX-2153C (Subramanian Rebuttal) at A. 344-46, 530, 534-35, 537-58.

²⁹² CX-99/RX-2 (the ‘517 patent) at col. 25:7-11.

m. "A chunk of input data being programmed into the memory system" (claims 12 and 13)

SanDisk asserts that the claim term "a chunk of input data being programmed into the memory system" should be construed as "a quantity of information, typically several bytes, to be programmed into the plurality of memory cells."²⁹³ ST asserts that the term should be construed as "N * L bits of user data, where N is the number of addressed cells and L is the number of bits per cell."²⁹⁴ Staff asserts that the claim term should be construed to require "several bytes of data" to be programmed into the memory system.²⁹⁵

SanDisk asserts that its claim construction is consistent with the plain meaning of the term, which is also consistent with the way the term is used in the specification.²⁹⁶

According to Staff, the claim term "chunk of input data" was also at issue in the 526 investigation. Staff asserts that, because the '517 specification uses the phrase in the same way as the '338 patent, the claim term should be interpreted the same.²⁹⁷

ST asserts that Judge Luckern construed "chunk of data" in claim 27 of the '338 patent to be "the final target memory states for the cells being programmed."²⁹⁸ According to ST, there is no reason to depart from Judge Luckern's claim construction with respect to "chunk of input data" in claims 12-14 of the '517 patent because these claims were expressly patterned after claim 27 of the

²⁹³ CIB 20.

²⁹⁴ RIB 12 citing RDX-67.

²⁹⁵ SIB 39 citing CX-99/RX-2 (the '517 patent) at col. 3:57-58, 28:8-10.

²⁹⁶ CIB 20 citing CX-2229C (Rhyne Direct) at Q. 529-31 ; CX-99/RX-2 (the '517 patent) at col. 3:56-58, 28:8-11.

²⁹⁷ SIB 39; SRB 19.

²⁹⁸ RIB 13 citing CX-372C (the 526 ID) at 21.

'338 patent.²⁹⁹ ST asserts that its claim construction is consistent with the plain meaning of the term, which is also consistent with the way the term is used in the specification and that a person of ordinary skill in the art would understand the claim term to require user data, not status flags.³⁰⁰

During the prehearing conference, the undersigned informed the parties that the undersigned intended to adopt the Commission's claim construction from the 526 investigation.³⁰¹ As this disputed claim term, which is in the '517 patent, is being used similarly as it was used in the '338 patent,³⁰² the undersigned agrees that the claim construction adopted for this claim term in the 526 investigation should also be adopted here. In the 526 investigation, Judge Luckern stated that the term "'chunk of data' is typically several bytes of data."³⁰³

Accordingly, the phrase **"a chunk of input data being programmed into the memory system"** in claims 12 and 13 is construed to require: **"several bytes of data to be programmed into the memory system."**

n. **"Comparing the threshold levels of the plurality of cells with the chunk of input data" (claim 13)**

SanDisk asserts that the claim term "comparing the threshold levels of the plurality of cells with the chunk of input data" should be construed as "requiring determining when the threshold levels of the plurality of cells have reached the desired threshold level ranges corresponding to the

²⁹⁹ See CX-103/RX-4 (the '517 prosecution history) at SDITC-II 12567/ST560-H 17074.

³⁰⁰ RIB 13 citing RX-1801 (Subramanian Direct) at 140-42; RX-2153C (Subramanian Rebuttal) at 124-27.

³⁰¹ Bullock, Tr. 20 (December 1, 2006 prehearing conference). See *Epcon Gas Sys., Inc. v. Bauer Compressors, Inc.*, 279 F.3d 1022, 1030 (Fed. Cir. 2002) ("*Epcon*") (the same term or phrase should be interpreted consistently where it appears in claims of common ancestry).

³⁰² It should be noted that, although the '338 patent and the '517 patent are not literally related, the specifications are identical in relevant part. SRB 19 citing CX-2229C (Rhyne Direct) at 26; CX-103/RX-4 (the '517 prosecution history) at SDITC-II 12566-67/ST560-H 17073-74.

³⁰³ CX-372C (the '526 Initial Determination) at 20.

data they are to store, *i.e.* the chunk of input data.”³⁰⁴ ST asserts that the term should be construed as “comparing the threshold level of each memory cell in the plurality of addressed cells against its corresponding bit in the chunk of input data.”³⁰⁵ Staff agrees with ST.³⁰⁶

SanDisk asserts that, while this claim term requires a comparison to be made, the comparison does not need to be direct; therefore, a comparator structure is not required. According to SanDisk, the claim limitation merely requires the step of comparing and does not recite any particular circuitry or structure used to achieve the comparison.³⁰⁷ In other words, SanDisk asserts that no particular structure is required by this method step.

ST asserts that the plain language of the claim term requires that the “threshold levels of the plurality of cells” be compared against the “chunk of input data.” According to ST, the specification explains that the threshold level of each cell in the plurality is assigned a bit value based upon the threshold level range in which it lies. One or more bits of user data will be stored for each cell, which collectively comprises the chunk of input data. After each pulse of appropriate voltage conditions, a verification is performed by reading the data bits out of each memory cell in the plurality and comparing them bit by bit against each bit of user data in the chunk of input data.³⁰⁸ In addition, ST counters SanDisk’s construction because it insists that no particular structure is

³⁰⁴ CIB 20-21 citing CX-2229C (Rhyne Direct) at Q. 537.

³⁰⁵ RIB 13 citing RDX-68.

³⁰⁶ SIB 39 citing CX-99/RX-2 (the ‘517 patent) at Fig. 23(5); col. 28:66-29:2.

³⁰⁷ CIB 21.

³⁰⁸ RIB 13-14 citing CX-99/RX-2 (the ‘517 patent) at Figs. 23-24; col 28:39-29:28; RX-1801 (Subramanian Direct) at 143-44; RX-2153C (Subramanian Rebuttal) at A. 568-72.

required, which is contrary to the specification.³⁰⁹ Staff agrees with ST.³¹⁰

The undersigned finds ST and Staff's arguments to be persuasive. The specification clearly states that this claim limitation requires comparing the data bits out of each memory cell in the plurality bit by bit against each bit of user data in the chunk of input data.³¹¹ In addition, the specification describes particular circuitry used to perform this comparison:

In each cell compare module such as the module 1701, the L read bits (L=number of binary bits encoded for each cell) are compared bit by bit with the corresponding program data bits.³¹²

This comparison is also shown in Figure 24, which is described in the specification as showing:

a "read data bit" produced by read circuits is compared by XOR gates against a "write data bit" produced from the read/program latches and shift registers 190 where the "chunk of input data" is stored.³¹³

These passages confirm that the chunk of input data is compared bit by bit with the threshold levels read from the plurality of addressed memory cells.

Accordingly, the phrase **"comparing the threshold levels of the plurality of cells with the chunk of input data"** in claim 13 is construed to mean: **"comparing the threshold level of each memory cell in the plurality of addressed cells against its corresponding bit in the chunk of input data."**

o. **"Cache memory" (claim 14)**

SanDisk asserts that the claim term "cache memory" should be construed as "any memory,

³⁰⁹ RRB 8 citing RX-1801C (Subramanian Direct) at Ans. 473-76; RX-2153C (Subramanian Rebuttal) at 568-72.

³¹⁰ SIB 39.

³¹¹ CX-99/RX-2 (the '517 patent) at Fig. 23(5); col. 28:66-29:2.

³¹² CX-99/RX-2 (the '517 patent) at col. 29:14-17.

³¹³ CX-99/RX-2 (the '517 patent) at col. 28:59-29:5.

distinct from the flash memory array, that is used to speed up the performance of the system by temporarily storing data to be programmed into memory cells.”³¹⁴ ST asserts that the term should be construed as “memory used to insulate the Flash memory device from enduring too many program/erase cycles allowing data to be operated on several times in the cache before being committed to the Flash memory.”³¹⁵ Staff asserts that the claim term should be construed by its ordinary meaning, which is “memory used to temporarily store data so as to speed up an operation.”³¹⁶

SanDisk asserts that its claim construction is consistent with the plain meaning of the term, which is also consistent with the way the term is used in the specification.³¹⁷ Staff also asserts that its claim construction is consistent with the plain meaning of the term, which is also consistent with the way the term is used in the specification.³¹⁸ ST asserts that the applicants defined “cache memory” as “novel” and “unlike . . . traditional caches.”³¹⁹ Therefore, ST asserts that the applicants acted as their own lexicographers in giving “cache memory” a special meaning for purposes of claim 14.³²⁰

³¹⁴ CIB 21.

³¹⁵ RIB 14 citing RDX-69.

³¹⁶ SIB 40 citing CX-2229C (Rhyne Direct) at 151-52; Subramanian, Tr. 1349; CX-99/RX-2 (the ‘517 patent) at col. 14:47-61, 2:44-54.

³¹⁷ CIB 21 citing CX-2229C (Rhyne Direct) at Q. 540-41; Subramanian, Tr. 1349; CX-99/RX-2 (the ‘517 patent), col. 14:46-61; 17:56-61; CX-1020 (Microsoft Press Computer Dictionary) at SDITC-II-067502-067508.

³¹⁸ SIB 40 citing CX-99/RX-2 (the ‘517 patent), col. 14:47-61; col. 2:44-54.

³¹⁹ RIB 14-15 citing CX-99/RX-2 (the ‘517 patent), col. 15:26-31 (“To overcome this problem, a cache memory is used in a novel way to insulate the Flash EEPROM memory device from enduring too many program/erase cycles. The primary function of the cache is to act on writes to the Flash EEPROM memory and not on reads of the Flash EEPROM memory, unlike the case with traditional caches.”)

³²⁰ RIB 14 citing *Boss Control, Inc. v. Bombardier Inc.*, 410 F.3d 1372, 1376-77 (Fed. Cir. (continued...))

The undersigned does not find ST's arguments to be persuasive. While the specification does use the term "cache memory" and "novel" in the same sentence, when reading the terms in context, there is no indication that the applicants were being their own lexicographers by assigning a particular meaning to the term "cache memory," other than its plain and ordinary meaning. Rather, the applicants were merely stating that "cache memory is *used* in a novel way."³²¹ The specification states that:

Cache memory is generally used to speed up the performance of systems having slower access devices.³²²

This is consistent with the plain meaning of the claim term, as testified by both SanDisk's and ST's experts.³²³

Accordingly, the phrase "**cache memory**" in claim 14 is construed to mean: "**memory used to temporarily store data so as to speed up an operation.**"

B. Infringement

SanDisk asserts that ST's NAND (SLC and MLC), [] flash memories and systems containing such chips infringe claim 1, 6-8, 10 and 12 of the '517 patent. SanDisk also asserts that ST's MLC NAND, [] chips infringe claims 3 and 5 of the '517 patent, while the [] also infringes claims 13 and 14 of the '517 patent.³²⁴ Furthermore, SanDisk asserts

³²⁰(...continued)

2005) ("*Boss Control*"); *Abraxis Bioscience, Inc. v. Mayne Pharma. (USA)*, 467 F.3d 1370, 1376 (Fed. Cir. 2006) ("*Abraxis*"); *Chef Am., Inc. v. Lamb-Weston, Inc.*, 358 F.3d 1371, 1374 (Fed. Cir. 2004) ("*Chef America*").

³²¹ CX-99/RX-2 (the '517 patent), col. 15:26-31 (emphasis added).

³²² CX-99/RX-2 (the '517 patent), col. 14:47-61.

³²³ CX-2229C (Rhyne Direct) at 151-52; Subramanian, Tr. 1349.

³²⁴ CIB 34 citing CDX-II 103. The specific products alleged to infringe include the: 512 Mb F12 NAND, 256 Mb F12 NAND, 128 Mb F90 NAND, 256 Mb F90 NAND, 512 Mb F90 NAND
(continued...)

that ST's accused products contributorily infringe the asserted method claims of the '517 patent, and that ST induced infringement of the '517 patent.³²⁵

ST asserts that the none of its accused NAND or NOR products infringe any asserted claims of the '517 patent.³²⁶ ST also asserts that SanDisk failed to prove either contributory or induced infringement.³²⁷

Staff asserts that ST's NAND products infringe claims 1, 3, 5, 6, 7, 8, and 10 of the '517 patent; however, Staff asserts that ST's NAND products, do not infringe claims 12, 13, and 14 of the '517 patent. In addition, Staff asserts that ST's NOR products do not infringe any of the asserted claims of the '517 patent.³²⁸ Furthermore, Staff agrees that ST's sale of flash memory chips, and in particular, ST's sales of NAND chips for use in products such as flash cards and USB drives, indirectly infringe the asserted claims of the '517 patent.³²⁹

1. Claim 1

- a. Preamble (A method of operating an EEprom system having memory cells that individually include an electrically floating gate carrying a charge level that is alterable in response to appropriate voltage conditions being applied to the cell in order to set a variable threshold level thereof into a range that is determinable by reading the cell, said method comprising)**

SanDisk asserts that ST's flash memories meet all the limitations of the preamble of claim 1 of the '517 patent because []

³²⁴(...continued)

(small page), 512 Mb F90 NAND (large page), 1 Gb F90 NAND, 2 Gb F90 NAND, 4 Gb F90 MLC NAND, 2 Gb F70 NAND, and 4 Gb F70 NAND.

³²⁵ CIB 40-41.

³²⁶ RIB 29-41.

³²⁷ RIB 41-44.

³²⁸ SIB 47; SRB 22-23.

³²⁹ SIB 53.

] ³³²

ST does not directly address whether its accused chips practice the preamble, other than stating that none of its NOR or NAND products practice claim 1 of the '517 patent because of other claim limitations and its contributory and induced infringement arguments.³³³

Staff asserts that, although ST's accused chips, by themselves, are not a "method of operating an EEPROM system," the evidence shows that ST's chips are used as part of such EEPROM systems, which is particularly true for products that ST produces itself, *i.e.* flash cards. Therefore, Staff asserts that ST's accused chips indirectly infringe claim 1.³³⁴

The undersigned agrees with Staff that, ST's NOR and NAND chips, by themselves, do not constitute a "method of operating an EEPROM system." The evidence shows, however, that ST's NOR and NAND chips are used as part of such EEPROM systems, such as flash cards that are produced by ST itself, which is discussed more fully in the indirect infringement section below.³³⁵ Therefore, the undersigned finds that ST indirectly infringes the preamble of claim 1 of the '517 patent.

³³⁰ CIB 34 citing CFF 2008-11, 2194-2202, 2222, 2276-78.

³³¹ CIB 34-35 citing CFF 2223-24, 2312-16, 2276-82.

³³² CIB 35 citing CFF 2225-73, 2282-2311.

³³³ RIB 29-44.

³³⁴ SIB 48.

³³⁵ *See infra*, Section V(B)(11).

- b. **First Limitation (applying said appropriate voltage conditions in parallel to a plurality of said memory cells, thereby to alter the charge levels on the floating gates of said plurality of memory cells)**

SanDisk asserts that ST's flash memories meet all the elements of the first limitation of claim 1 of the '517 patent because, [

] ³³⁶ Staff agrees with SanDisk that ST's accused products meet all the elements of the first limitation because [

] ³³⁷ ST does not directly address whether its accused chips practice the first limitation, other than based on its claim construction and stating that none of its NOR or NAND products practice claim 1 of the '517 patent because of other claim limitations and its contributory and induced infringement arguments. ³³⁸

Both SanDisk and Staff counter ST's arguments as being based on ST's faulty claim construction requiring fixed programming pulses and "hot electron injection" programming. ³³⁹ The undersigned rejected ST's claim construction argument above. Therefore, ST's arguments are also rejected here and the undersigned finds that ST's accused products practice the first limitation of claim 1 of the '517 patent.

³³⁶ CIB 35 citing CFF 2312-32, 2338-39, 2350-81.

³³⁷ SIB 48 citing CX-2229C (Rhyne Direct) at 175-79, 223-24, 274-75.

³³⁸ RIB 29-44.

³³⁹ CIB 35; SIB 48-49.

- c. **Second Limitation (determining the threshold level ranges in which individual ones of said plurality of memory cells lie, and)**

(1) ST NAND

SanDisk asserts that ST's NAND flash memories meet all the elements of the second limitation of claim 1 of the '517 patent because, [

]³⁴⁰

Staff agrees with SanDisk that ST's accused NAND products infringe this claim limitation because [

341

]

³⁴⁰ CIB 36 citing CFF2382-2432, 2228-2273.

³⁴¹ SIB 50 citing Subramanian, Tr. 1378-81; SRB 25 citing CX-2229C (Rhyne Direct) at 181-

[342

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ST asserts that its accused NAND products do not perform the “determining” step because

[

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³⁴² SIB 50-51 citing RX-2153C (Subramanian Rebuttal) at 250-58; Subramanian, Tr. 1378-81, 1471-84.

³⁴³ SRB 25.

³⁴⁴ SRB 26 citing Subramanian, Tr. 1471-84.

] ³⁴⁶

SanDisk counters ST's arguments, asserting that ST's own documents and witnesses contradict ST's argument. [

347

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] ³⁵⁰

ST counters Staff's arguments, asserting that Staff is mistaken as to how ST's accused NAND products assign bit values to cells. According to ST, ST chooses to design its NAND to be cheap and easy to manufacture. [

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³⁴⁵ RIB 35-36 citing RX-2157C (Maccarrone Rebuttal) at A. 74, 84; RDX-139; RX-2153C (Subramanian Rebuttal) at A. 1252; Rhyne, Tr. 2020-22; Subramanian, Tr. 1406; RDX-172-002.

³⁴⁶ RIB 35-37.

³⁴⁷ CIB 36 citing Subramanian, Tr. 1148, 1307, 1377.

³⁴⁸ CRB 15-16 citing JX-66C (Mastrangelo Dep) at 54, 58.

³⁴⁹ CRB 16-17 citing CFF1054-1056.

³⁵⁰ CIB 36 citing CFF 2228-73, 2415-32; CRB 15-17.

[
]³⁵²

The undersigned finds SanDisk's and Staff's arguments to be persuasive. Based on a review of the evidence, the undersigned finds that, [

353

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] ³⁵⁶ The majority of ST's arguments are based on their claim construction that the "determining" limitation requires measuring the threshold level of each cell, which was rejected above.

The undersigned does not, however, find SanDisk's "margin" arguments to be persuasive. As noted above, the undersigned rejected SanDisk's claim construction argument that the

³⁵¹ RRB 12 citing Subramanian, Tr. 1394; RX-1801C (Subramanian Direct) at A. 764-67; RDX-96.02, 96.03, 96.07.

³⁵² RRB 12 citing RX-2253 (Subramanian Rebuttal) at A. 1266 [check if 2153 or 2253].

³⁵³ Other factors that affect the read operation in ST's accused NAND products include mobility, oxide capacitance, channel width, and channel length RX-2157C (Maccarrone Rebuttal) at A. 80, p. 15.

³⁵⁴ Subramanian, Tr. 1406; RDX-172-2C; Rhyne, Tr. 1984-86.

³⁵⁵ RX-2153C (Subramanian Rebuttal) at 250-58; Subramanian, Tr. 1378-81, 1471-84.

³⁵⁶ See Section V(A)(2)(g).

“determining” limitation included “margin³⁵⁷ing.” Regardless of whether ST uses “margin³⁵⁷ing,” however, the undersigned finds that ST’s accused NAND products practice the “determining” limitation of claim 1 of the ‘517 patent.

Accordingly, the undersigned finds that ST’s accused NAND products practice the second limitation of claim 1 of the ‘517 patent.

(2) ST NOR

SanDisk asserts that ST’s NOR flash memories meet all the elements of the second limitation of claim 1 of the ‘517 patent because, [

]³⁵⁸

[

359

]

³⁵⁷ See Section V(A)(2)(g).

³⁵⁸ CIB 37 citing CFF2447-2563, 2285, 2298-99.

³⁵⁹ RIB 30 citing RX-2155C (Villa Direct) at a. 67, p. 12; RRB 12 citing Rhyne, Tr. 1949-50, 1954-56, 2390.

] ³⁶³

Staff agrees with ST that [

] ³⁶⁴ According to Staff, this method does not appear to be the same, or the equivalent, to determining the threshold level ranges of the cell, as construed above. ³⁶⁵

SanDisk counters ST's arguments, asserting that ST is avoiding infringement by creating confusion regarding the [

]

³⁶⁰ RIB 32 citing Rhyne, Tr. 1917-18.

³⁶¹ RIB 33 citing RX-2153C (Subramanian Rebuttal) at A. 1257-60, p. 351-52; RDX-159.

³⁶² RIB 34 citing Subramanian, Tr. 1409-11; RDX-172-2C (*see also* Appendix D).

³⁶³ RIB 34 citing Rhyne, Tr. 1970, 1985, 2022, 2075.

³⁶⁴ SIB 48, 50 citing RX-2153C (Subramanian Rebuttal) at 349.

³⁶⁵ SIB 50.

³⁶⁶ CRB 17.

[]³⁶⁷

In addition, SanDisk asserts that the testimony of ST's experts contradicts ST's arguments.³⁶⁸

Specifically, SanDisk asserts that Dr. Subramanian admitted that in ST's NOR products, [

369

] ³⁷⁰ Alternatively, SanDisk asserts that ST's accused NOR products infringe by the doctrine of equivalents.³⁷¹

The undersigned agrees with ST and Staff that SanDisk has not shown, by a preponderance of evidence, that ST's accused NOR products, practice the "determining" limitation of claim 1 of the '517 patent. The evidence shows that ST's NOR chips determine the memory state of the cell

[]

³⁶⁷ CRB 19.

³⁶⁸ CIB 37 citing Subramanian, Tr. 1307.

³⁶⁹ CRB 17-18 citing CFF 2559-61, 2595-2613, 2624-36.

³⁷⁰ CRB 19 citing CFF 1054-56.

³⁷¹ CIB 37 citing CFF2503-2512, 2556-2563. Although SanDisk raises a doctrine of equivalents argument, the issue was not adequately briefed in the post-hearing brief or post-hearing reply brief. A single sentence alleging that the accused products infringe by the doctrine of equivalents, with a reference to more detailed arguments in the proposed findings of facts, is insufficient. Therefore, SanDisk's doctrine of equivalents argument is rejected. A reasonable page-limit for briefs was imposed on the parties in this investigation to narrow the number of issues that needed to be decided by the undersigned. The undersigned did not intend the parties to use the findings of facts for the arguments they chose not to elaborate on in their briefs.

[

] ³⁷² In addition, SanDisk's "margin" argument is also rejected, as the undersigned did not include such a requirement in the claim construction for "determining."³⁷³

Accordingly, the undersigned finds that SanDisk has not proved, by a preponderance of the evidence, that ST's accused NOR products practice the "determining" limitation of claim 1 of the '517 patent.

- d. **Third Limitation (terminating said application of appropriate voltage conditions to individual ones of said plurality of memory cells upon their being determined to have reached desired threshold level ranges while continuing to apply said appropriate voltage conditions to others of said plurality of cells)**

SanDisk asserts that ST's flash memories meet all the elements of the third limitation of claim 1 of the '517 patent because, [

374

] ³⁷⁵

ST asserts that its accused products do not infringe the "terminating" limitation based on its

³⁷² RX-2153C (Subramanian Rebuttal) at 349.

³⁷³ See Section V(A)(2)(g).

³⁷⁴ CIB 37 citing CFF2564-2648.

³⁷⁵ SIB 49 citing CX-2229C (Rhyne Direct) at 185-86, 226-28, 277-79.

claim construction because in all of its accused products, [

376

377

] ³⁷⁸

Both SanDisk and Staff counter ST's arguments regarding the "terminating" limitation as being based on ST's faulty claim construction requiring preventing any further alternation of charge on the floating gate of an inhibited cell, *i.e.* that the cells must prevent program disturb.³⁷⁹ The undersigned rejected ST's claim construction argument above. Therefore, ST's arguments are also rejected here and the undersigned finds that ST's accused products practice the "terminating" limitation of claim 1 of the '517 patent.

Both SanDisk and Staff counter ST's arguments regarding the "continuing" limitation as being based on ST's faulty claim construction requiring applying the identical programming pulse

³⁷⁶ RIB 39 citing Rhyne, Tr. 2037-38; RX-2153C (Subramanian Rebuttal) at A. 1279-82, p. 358; RX-2155C (Villa Direct) at A. 96, p. 21; RX-2157C (Maccarrone Rebuttal) at A. 92-94, p. 14-18; RRB 14-15.

³⁷⁷ RRB 14.

³⁷⁸ RIB 38 citing RX-2153C (Subramanian Rebuttal) at A. 1223-24, p. 340-41; RX-2155C (Villa Direct) at A.112, p. 24; RX-2156C (Sali Direct) at A. 43, p. 6; RX-2157C (Maccarrone Rebuttal) at A. 86, p. 16; RRB 11-12.

³⁷⁹ CRB 20; SIB 49; SRB 23.

during each successive pulse of a program operation.³⁸⁰ The undersigned rejected ST's claim construction argument above. Therefore, ST's arguments are also rejected here and the undersigned finds that ST's accused products practice the "continuing" limitation of claim 1 of the '517 patent.

Accordingly, the undersigned finds that ST's accused products practice the third limitation of claim 1 of the '517 patent.

e. Fourth Limitation (until all of the plurality of cells are determined to have reached their desired threshold level ranges)

SanDisk asserts that ST's flash memories meet all the elements of the fourth limitation of claim 1 of the '517 patent because [

] ³⁸¹ Staff agrees with SanDisk that ST's accused products meet all the elements of the fourth limitation.³⁸²

ST asserts that its accused NAND products do not perform this limitation because [

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384

]

³⁸⁰ CRB 19 citing CFF 771, 2582-85; SRB 23.

³⁸¹ CIB 38 citing CFF 2649-2686.

³⁸² SIB 49 citing CX-2229 (Rhyne Direct) at 186-88, 228-29, 279-80.

³⁸³ RIB 29-30 citing Rhyne, Tr. 1763-64; RRB 11.

³⁸⁴ RRB 15.

[

]³⁸⁵

Both SanDisk and Staff counter ST's arguments as being based on faulty claim construction of what constitutes a desired range.³⁸⁶ The undersigned rejected ST's claim construction argument above. Therefore, ST's arguments are also rejected here and the undersigned finds that ST's accused products practice the fourth limitation of claim 1 of the '517 patent.

f. Conclusion

Accordingly, the undersigned finds that SanDisk has proved, by a preponderance of the evidence that ST's accused NAND products infringe each and every limitation of claim 1 of the '517 patent. The undersigned finds, however, that SanDisk has not proved, by a preponderance of the evidence, that ST's accused NOR products infringe each and every limitation of claim 1 of the '517 patent.

2. Claim 3 (The method of claim 1, wherein there are more than two threshold level ranges)

SanDisk asserts that ST's flash memories meet all the elements of dependent claim 3 of the '517 patent because [

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]

³⁸⁵ RRB 15 citing RX-2155C (Villa Rebuttal) at A. 143; RFF1426-31.

³⁸⁶ CIB 38; CRB 20; SIB 49.

³⁸⁷ CIB 38 citing CFF 2687-2693.

³⁸⁸ RIB 39 citing RX-2153 (Subramanian Rebuttal) at A. 1383-1428, p. 380-86; RRB 15.

[

]³⁸⁹

As ST has not provided any additional arguments other than the ones proposed above for claim 1, which were rejected above, the undersigned finds that ST's accused MLC NAND products also infringe dependent claim 3 of the '517 patent.

3. Claim 5 (The method of claim 1, wherein the threshold level ranges are separated by more than one breakpoint threshold level, thereby to provide more than two non-overlapping threshold level ranges)

SanDisk asserts that ST's flash memories meet all the elements of dependent claim 5 of the '517 patent because [

]³⁹⁰ ST asserts that, as claims 3, 5, 6, 7, 8, 10, and 11 depend from claim 1, its accused products do not infringe this dependent claim for the same reasons claim 1 is not infringed.³⁹¹ Staff asserts that ST does not contend that the accused chips do not satisfy the additional limitations in claim 5; therefore, any version of ST's F90 4Gb MLC NAND chips that infringe claim 1 also infringe claim 5.³⁹²

As ST has not provided any additional arguments other than the ones proposed above for claim 1, which were rejected above, the undersigned finds that ST's accused MLC NAND products also infringe dependent claim 5 of the '517 patent.

4. Claim 6 (The method of claim 1, wherein said desired threshold level ranges include an erased threshold level range)

SanDisk asserts that ST's flash memories meet all the elements of dependent claim 6 of the

³⁸⁹ SIB 51; SRB 26.

³⁹⁰ CIB 38 citing CFF 2694-99.

³⁹¹ RIB 39 citing RX-2153 (Subramanian Rebuttal) at A. 1383-1428, p. 380-86; RRB 15.

³⁹² SIB 51; SRB 26.

'517 patent because [

] ³⁹³

ST asserts that, as claims 3, 5, 6, 7, 8, 10, and 11 depend from claim 1, its accused products do not infringe this dependent claim for the same reasons claim 1 is not infringed.³⁹⁴ In addition, ST asserts that its accused products do not practice the additional limitation in claim 6 because [

395

]

Staff counters ST's arguments regarding claim 6 as being based on incorrect claim construction. According to Staff, all that claim 6 requires is single or multi-level cells with an erased range. Therefore, Staff asserts that claim 6 is infringed by all of ST's accused NAND products.³⁹⁶

The undersigned agrees with SanDisk and Staff that claim 6 covers single level cells with an erased range, which is consistent with the claim construction adopted above.³⁹⁷ As ST has not provided any other arguments, which have already been rejected above, the undersigned finds that ST's accused NAND products also infringe dependent claim 6 of the '517 patent.

³⁹³ CIB 39 citing CFF 2700-04.

³⁹⁴ RIB 39 citing RX-2153 (Subramanian Rebuttal) at A. 1383-1428, p. 380-86.

³⁹⁵ RIB 39 citing RX-2153 (Subramanian Rebuttal) at A. 1399-1403, p. 382-84; Rhyne, Tr. 1765.

³⁹⁶ SIB 51-52 citing CX-2229C (Rhyne Direct) at 190-91, 231-32, 281-82; SRB 26.

³⁹⁷ See *supra*, section V(A)(2)(j); CX-2229C (Rhyne Direct) at 190-91, 231-32, 281-82.

5. **Claim 7 (The method of claim 1, wherein the array of memory cells are grouped into blocks of cells wherein the threshold levels of cells within a selected one of the blocks are changed together to a single given threshold level range prior to applying said appropriate voltage conditions in parallel to the plurality of cells within said one block)**

SanDisk asserts that ST's flash memories meet all the elements of dependent claim 7 of the '517 patent because [

] ³⁹⁸ ST asserts that, as claims 3, 5, 6, 7, 8, 10, and 11 depend from claim 1, its accused products do not infringe this dependent claim for the same reasons claim 1 is not infringed. ³⁹⁹ Staff asserts that ST does not contend that the accused chips do not satisfy the additional limitations in claim 7; therefore, any products that infringe claim 1 also infringe claim 7. ⁴⁰⁰

As ST has not provided any additional arguments other than the ones proposed above for claim 1, which were rejected above, the undersigned finds that ST's accused NAND products also infringe dependent claim 7 of the '517 patent.

6. **Claim 8 (The method of claim 7, wherein individual ones of said blocks include a specific number of memory cells and said plurality of memory cells to which said appropriate voltage conditions are applied in parallel are less than said specific number, and additionally comprising repeating for another plurality of cells within said one block said applying, determining and terminating operations)**

SanDisk asserts that ST's flash memories meet all the elements of dependent claim 8 of the '517 patent [

] ⁴⁰¹ ST asserts that, as claims 3, 5, 6, 7, 8, 10, and 11 depend from claim 1, its accused products do not infringe this

³⁹⁸ CIB 39 citing CFF2705-39.

³⁹⁹ RIB 39 citing RX-2153 (Subramanian Rebuttal) at A. 1383-1428, p. 380-86; RRB 15.

⁴⁰⁰ SIB 52; SRB 26.

⁴⁰¹ CIB 39 citing CFF 2740-51.

dependent claim for the same reasons claim 1 is not infringed.⁴⁰² Staff asserts that ST does not contend that the accused chips do not satisfy the additional limitations in claim 8; therefore, any products that infringe claim 1 also infringe claim 8.⁴⁰³

As ST has not provided any additional arguments other than the ones proposed above for claim 1, which were rejected above, the undersigned finds that ST's accused NAND products also infringe dependent claim 8 of the '517 patent.

7. Claim 10 (The method of any one of claims 1-9, carried out on a single integrated circuit chip)

SanDisk asserts that ST's flash memories meet all the elements of dependent claim 10 of the '517 patent because[]⁴⁰⁴

ST asserts that, as claims 3, 5, 6, 7, 8, 10, and 11 depend from claim 1, its accused products do not infringe this dependent claim for the same reasons claim 1 is not infringed.⁴⁰⁵ Staff asserts that ST does not contend that the accused chips do not satisfy the additional limitations in claim 10; therefore, any products that infringe claim 1 also infringe claim 10.⁴⁰⁶

As ST has not provided any additional arguments other than the ones proposed above for claim 1, which were rejected above, the undersigned finds that ST's accused NAND products also infringe dependent claim 10 of the '517 patent.

⁴⁰² RIB 39 citing RX-2153 (Subramanian Rebuttal) at A. 1383-1428, p. 380-86; RRB 15.

⁴⁰³ SIB 52; SRB 26.

⁴⁰⁴ CIB 39 citing CFF 2752-56.

⁴⁰⁵ RIB 39 citing RX-2153 (Subramanian Rebuttal) at A. 1383-1428, p. 380-86; RRB 15.

⁴⁰⁶ SIB 52; SRB 26.

8. **Claim 12 (The method of claim 1 wherein the desired ones of said threshold level ranges reached by applying appropriate voltage conditions to the plurality of memory cells correspond to a chunk of input data being programmed into the memory system)**

SanDisk asserts that ST's flash memories meet all the elements of dependent claim 12 of the '517 patent because, [

] ⁴⁰⁷

ST asserts that its products do not infringe claim 12 for same reasons it does not infringe claim 1. In addition, ST asserts that its accused products do not program a "chunk of input data" into memory cells because [

] ⁴⁰⁸

Staff agrees with ST that ST's accused NAND products do not practice the additional limitation in claim 12 because ST's NAND products do not store a "chunk of data." Staff agrees that ST's NAND products use [] to indicate whether the cell should be programmed. According to Staff, the use of [] is substantially different from suing a "chunk of input data."⁴⁰⁹ Staff asserts that this was also the conclusion reached by Judge Luckern in the 526 investigation.⁴¹⁰

SanDisk counters both ST's and Staff's arguments. SanDisk asserts that both ST and Staff are confusing the "means for temporarily storing" element in claim 27 of the '338 patent, with the requirements in claim 12 of the '517 patent. According to SanDisk, claim 12 of the '517 patent has no requirement that the EEPROM system store the "chunk of input data." Rather, SanDisk asserts that

⁴⁰⁷ CIB 39 citing CFF 2757-2817.

⁴⁰⁸ RIB 40 citing CX-372C (the 526 ID) at 77; RX-2153C (Subramanian Rebuttal) at A. 1434-58, p. 387-98; RX-2157C (Maccarrone Direct) at A. 105-07, p. 19; Rhyne, Tr. 2042-45, 2142-45; RX-2155C (Villa Direct) at A. 137-41, p. 29-30; RX-2156 (Sali Direct) at A. 32-39, p. 4-6; CX-32C (W8DL design review) at 41560; RX-1670C (W9EL design review) at ST560 41952; RRB 15.

⁴⁰⁹ SIB 52 citing RX-2153C (Subramanian Direct) at 395-98; SRB 26-27.

⁴¹⁰ SIB 52 citing CX-372C (the 526 ID) at 67-75 (use of status flags in ST's NAND did not satisfy the "means for temporarily storing a chunk of data" limitation).

the claim only requires that the “desired threshold level ranges reached by applying appropriate voltage conditions” correspond “to a chunk of input data being programmed into the memory system []⁴¹¹ Alternatively, SanDisk asserts that, even if ST’s accused products use [] ST’s products infringe under the doctrine of equivalents.⁴¹²

The undersigned agrees with ST’s and Staff’s arguments that claim 12 requires that a “chunk of input data” be programmed into memory cells and that ST’s products [] which is not the same,⁴¹³ nor the equivalent.⁴¹⁴ This is consistent with the finding made in the 526 investigation.⁴¹⁵ While SanDisk argues that the ‘517 patent does not require that the “chunk of input data” be stored as was required by the ‘338 patent, and that the ‘517 only requires a “correspondence,” SanDisk has not shown that there is such a “correspondence” by a preponderance of the evidence.

Accordingly, SanDisk has not shown, by a preponderance of the evidence, that ST’s accused products infringe each and every limitation of claim 12 of the ‘517 patent.

⁴¹¹ CRB 20-21 citing CX-99/RX-2 (the ‘517 patent) at col. 31:40-44.

⁴¹² CIB 40 citing CFF 2788-2791.

⁴¹³ RX-2153C (Subramanian Rebuttal) at A. 1434-58, p. 387-98; RX-2157C (Maccarrone Direct) at A. 105-07, p. 19; Rhyne, Tr. 2042-45, 2142-45; RX-2155C (Villa Direct) at A. 137-41, p. 29-30; RX-2156 (Sali Direct) at A. 32-39, p. 4-6; CX-32C (W8DL design review) at 41560; RX-1670C (W9EL design review) at ST560 41952.

⁴¹⁴ SanDisk’s doctrine of equivalents analysis is rejected. *See* footnote 371.

⁴¹⁵ CX-372C (the 526 ID) at 77.

9. **Claim 13 (The method of claim 12, wherein the plurality of cells are determined to have reached the desired threshold level ranges by comparing the threshold levels of the plurality of cells with the chunk of input data)**

SanDisk asserts that ST's [] flash memory meets all the elements of dependent claim 13 of the '517 patent.⁴¹⁶

ST asserts that SanDisk waived asserting claim 13 against ST's NAND products, because the issue was not preserved in SanDisk's pre-hearing brief.⁴¹⁷ As for ST's NOR products, ST asserts that its products do not infringe for same reasons claims 1 and 12 do not infringe. Specifically, ST asserts that, based on its claim construction of the "determining" limitation, ST's accused products [

418

] ⁴¹⁹

Staff agrees with ST that ST's accused NAND products do not practice the additional limitation in claim 13 because [] as discussed above in claim 12.⁴²⁰

The undersigned determined above that SanDisk failed to prove, by a preponderance of the evidence, that ST's accused products infringe claim 12 of the '517 patent. Therefore, because claim 13 depends from claim 12, the undersigned finds that ST's accused products also do not infringe claim 13 of the '517 patent.

⁴¹⁶ CIB 40 citing CFF 2818-22; CRB 20.

⁴¹⁷ RIB 40 citing SanDisk's Prehearing Brief 247-48 and Ground Rule 8.2.

⁴¹⁸ RIB 40 citing RX-2153C (Subramanian Rebuttal) at A. 1464-78, p. 398-402.

⁴¹⁹ RIB 41 citing Rhyne, Tr. 2142-43; RRB 16.

⁴²⁰ SIB 52; SRB 26-27.

10. Claim 14 (The method of claim 13, wherein the chunk of input data is stored in a cache memory prior to being programmed into memory cells within the EEprom)

SanDisk asserts that ST's [] flash memory meets all the elements of dependent claim 14 of the '517 patent.⁴²¹

ST asserts that SanDisk waived asserting claim 14 against ST's NAND products, because the issue was not preserved in SanDisk's pre-hearing brief.⁴²² As for ST's NOR products, ST asserts that its products do not infringe for same reasons claims 1, 12, and 13 do not infringe. Specifically, ST asserts that, based on its claim construction of the "cache memory" limitation, this claim requires a memory used to insulate the flash memory device from enduring too many program/erase cycles allowing data to be operated on several times in the cache before being committed to the flash memory. ST asserts that Dr. Rhyne conceded that ST's [

] ⁴²³ In addition, ST asserts that its[

] ⁴²⁴

Staff agrees with ST that ST's accused NAND products do not practice the additional limitation in claim 14 because ST's NAND products [] as discussed above in claim 12.⁴²⁵

The undersigned does not find ST's argument persuasive, as the undersigned did not adopt ST's claim construction for "cache memory." The undersigned determined above, however, that

⁴²¹ CIB 40 citing CFF 2823-24; CRB 20.

⁴²² RIB 41 citing SanDisk's Prehearing Brief 248-49 and Ground Rule 8.2.

⁴²³ RIB 41 citing RX-2153C (Subramanian Rebuttal) at A. 1485, p. 402-03; CX-2229C (Rhyne Direct) at p. 286.

⁴²⁴ RIB 41 citing RX-1664C (W8DL design review) at ST560 41567-68; RX-2153C (Subramanian Direct) at A. 1492, p. 403-04.

⁴²⁵ SIB 52; SRB 26-27.

SanDisk failed to prove, by a preponderance of the evidence, that ST's accused products infringe claim 12 of the '517 patent. Therefore, because claim 14 depends from claim 12, the undersigned finds that ST's accused products also do not infringe claim 14 of the '517 patent.

11. Indirect Infringement

a. Induced Infringement

SanDisk asserts that ST induces infringement of the '517 patent. First, SanDisk asserts that ST knew of the '517 patent since at least October 2005. Second, SanDisk asserts that there is substantial evidence of direct infringement by ST's customers.⁴²⁶ SanDisk asserts that ST intended to cause the acts which constitute infringement because ST intended the accused products to be programmed and erased during normal use, qualification, and/or testing. SanDisk asserts that it is reasonable to infer that ST intends the ordinary use to occur and has taken active steps to encourage the use of its accused products in which those flash memories will be programmed, and in most cases, later erased and reprogrammed. According to SanDisk, ST markets its products for use in cell phones, removable storage media, set-top boxes, etc., and that ST instructs its customers how to design their products to perform the infringing commands.⁴²⁷

As to ST's MLC NOR products, SanDisk asserts that ST advertises these chips for use in storing data, as well as code, in cell phones.⁴²⁸ As to ST's NAND products, SanDisk asserts that ST advertises these chips as advantageous for applications that store code because the memory can be

⁴²⁶ CIB 41 citing CFF 3332-83.

⁴²⁷ CIB 41 citing CFF 3384-90.

⁴²⁸ CIB 41-42 citing CX-867 (ST website) at SDITC-II-153467; CX-868 (press release) at SDITC-II-168949; CX-2229C (Rhyne Direct) at Q. 1468.

erased and programmed.⁴²⁹ According to SanDisk, ST informs its customers on how to use the accused products to perform the commands which infringe the '517 patent, that is to be programmed, erased, and then re-programmed. Therefore, according to SanDisk, ST intends to cause the acts which constitute infringement.⁴³⁰

Staff agrees with SanDisk that ST's sale of flash memory chips indirectly infringe the asserted claims of the '517 patent.⁴³¹ Staff asserts that ST learned of the '517 patent, at the latest, when the complaint was filed, and that ST continued to produce and import the accused chips.⁴³² According to Staff, ST produces and sells flash memory cards and currently has approximately 100,000 in inventory in the United States. Staff asserts that the ordinary use of a flash memory card involves programming, and sometimes erasing, the card.⁴³³ In addition, Staff asserts that ST sells its chips to customers who incorporate them into other products, such as USB drives, and provides instructions to its customers on how to use the chips.⁴³⁴ Based on the above, Staff asserts that there is evidence of induced infringement.⁴³⁵

ST asserts that SanDisk has failed to prove an act of direct infringement by any third party or that ST was even aware of a single act of direct infringement by a third party.⁴³⁶ According to ST:

⁴²⁹ CIB 43 citing CX-827 (application note) at SDITC-II-153709.

⁴³⁰ CIB 42 citing CFF 3339, 3342-49, 3368, 3379, 3384-85, 3391, 3395-98, 3400, 3416-19, 3421-22, 3426.

⁴³¹ SIB 53-54.

⁴³² SIB 53 citing Casagrande, Tr. 1513-14; ST's Response to Second Amended Complaint at 1.

⁴³³ SIB 53 citing CX-2229C (Rhyne Direct) at 391; Casagrande, Tr. 1510; Napper, Tr. 961.

⁴³⁴ SIB 53 citing Subramanian, Tr. 1370-71; CX-2229C (Rhyne Direct) at 392-99, 401-07.

⁴³⁵ SIB 53 citing *Golden Blount, Inc. v. Robert H. Peterson Co.*, 438 F.3d 1354, 1362-63 (Fed. Cir. 2006) ("*Golden Blount*"); *Moleculon Research Corp. v. CBS, Inc.*, 793 F.2d 1261, 1272, (Fed. Cir. 1986) ("*Moleculon*").

⁴³⁶ RIB 43-44; RRB 17-18.

1) its flash memories alone cannot infringe the '517 patent;⁴³⁷ 2) it does not know into what products its customers may or may not integrate ST flash memory and does not know how, if at all, ST flash memory might be used in any particular customer's product;⁴³⁸ 3) when a customer buys an ST chip, it is the customer who decides what controller to use and what commands that controller can issue to the ST chip;⁴³⁹ 4) it has no knowledge, provides no assistance, and plays no role whatsoever in what distributors do after they purchase memory from ST;⁴⁴⁰ 5) its memories are commodity goods and memory customers design their product specifications before ever purchasing a memory product from ST;⁴⁴¹ and 6) it has never even suggested or encouraged any U.S. customer to perform any particular operation on an ST memory.⁴⁴²

SanDisk counters ST's arguments that SanDisk has failed to prove an act of direct infringement by a third party. According to SanDisk, the evidence shows direct acts of infringement in the U.S. by products that use the accused chips and that ST knew and promoted acts that constitute direct infringement.⁴⁴³

Staff also counters ST's arguments relying on *DSU* for the proposition that because it does not know how its customers use its chips, no specific intent can be found. According to Staff, at the very least, ST itself sells flash memory cards and it certainly knows that its own products operate in

⁴³⁷ RIB 43 citing Rhyne, Tr. 1732-33, 2047-49, 2052.

⁴³⁸ RIB 43 citing JX-5C (Matte Dep) at 47, 50-51, 92-93, 192-94, 210; JX-141C (Ponzanelli Dep) at 56, 110-11; JX-144C (Zhang Dep) at 132-33; JX-140C (Peyret Dep) at 73, 77-78, 126-27.

⁴³⁹ RIB 43 citing Rhyne, Tr. 2050-51, 2058.

⁴⁴⁰ RIB 43 citing JX-33C (Shopes Dep) at 44-45; JX-28C (Pecoraro Dep) at 69-70.

⁴⁴¹ RIB 43-44 citing JX-32C (Sheen Dep) at 102.

⁴⁴² RIB 44 citing Rhyne, Tr. 2068-70.

⁴⁴³ CRB 23 citing CFF3342-83, 3384-400, 3333, 3358, 3416-22, 3426, 3339-3449, 3395-98; CX-867 (ST website) at SDITC-II-153467; CX-868 (press release) at SDITC-II-168949; CX-2229C (Rhyne Direct) at A. 1468.

accordance with its own specification.⁴⁴⁴ With respect to ST's other products, Staff asserts that there is significant evidence that ST's customers use the chips as set out in ST's data sheets.⁴⁴⁵ Therefore, Staff asserts that this is a case where the product is intended to be used in a particular way, which is taught by the proffered instructions and which, when used, practices the claimed method.⁴⁴⁶

The required elements of a claim of induced infringement are: "(1) an act of direct infringement; (2) the accused infringer actively induced a third party to infringe the patent; and (3) the accused infringer knew or should have known that his actions would induce infringement."⁴⁴⁷ As for intent, it can be shown through circumstantial evidence.⁴⁴⁸

As to ST's accused NOR products, the undersigned did not find an act of direct infringement, which is required for the purposes of finding induced infringement. Accordingly, the undersigned finds that SanDisk has failed to prove that ST's accused NOR products induce infringement of the '517 patent.

As to ST's accused NAND products, the undersigned finds that the evidence shows that there has been an act of direct infringement, that ST actively induced third parties to infringe the patent, and that ST knew or should have known that its actions would induce infringement. ST learned of the '517 patent, at the latest, when this complaint was filed on January 10, 2006, and that ST continued to produce and import the accused chips, which includes a large inventory of chips in the

⁴⁴⁴ SRB 27 citing CX-2229C (Rhyne Direct) at 157-61, 391.

⁴⁴⁵ SRB 27 citing CFF 3450-3717.

⁴⁴⁶ SRB 27.

⁴⁴⁷ *Certain Flash Memory Circuits*, Comm'n Op. at 16.

⁴⁴⁸ *LaBounty*, 958 F.2d at 1076 ("[d]irect proof of wrongful intent is rarely available but may be inferred from clear and convincing evidence of the surrounding circumstances."); *Bristol-Myers*, 326 F.3d at 1239; *GFI Inc. v. Franklin Corp.*, 265 F.3d 1268, 1274 (Fed. Cir. 2001) ("*GFI*"); *Merck & Co. v. Danbury Pharmacal, Inc.*, 873 F.2d 1418, 1422 (Fed. Cir. 1989) ("*Danbury*").

United States.⁴⁴⁹ The ordinary use of a flash memory card involves programming, erasing, and reprogramming the flash memory card.⁴⁵⁰ ST itself produces flash memory cards and it also sells chips to customers who incorporate them into other products. While ST argues that it does not know what its customers do with the flash memory chips and that it is the customer who decides what controller to use with the chip, the evidence shows that ST's customers use the chips as set out in ST's data sheets and perform in the way they were intended to be used. Based on the above, the undersigned finds that SanDisk has proved that there is evidence of induced infringement with respect to ST's accused NAND products.

b. Contributory Infringement

SanDisk asserts that ST's accused products contributorily infringe the asserted claims of the '517 patent. SanDisk asserts that ST has known of the '517 patent since at least October 2006, when ST filed a complaint discussing the 07/337,566 application, from which the '517 patent ultimately issued. According to SanDisk, ST knows that, during ordinary use, products containing ST's accused products directly infringe various method claims of the '517 patent. ST asserts that each of the accused ST products is sold for use in practicing the patented method claims, and, in operation, practices a material part of the claimed method. According to SanDisk, ST specifically designs its accused products to be programmed, erased, and reprogrammed.⁴⁵¹

SanDisk asserts that there are no substantial non-infringing uses for the accused flash memory products because an accused ST product that is in the U.S. and includes flash memory is highly likely to be reprogrammed in the U.S. at some point, even if it was originally programmed

⁴⁴⁹ Casagrande, Tr. 1513-14; ST's Response to Second Amended Complaint at 1.

⁴⁵⁰ CX-2229C (Rhyne Direct) at 391; Casagrande, Tr. 1510; Napper, Tr. 961.

⁴⁵¹ CIB 40-41 citing CFF 3340-41, 3329.

outside the U.S.⁴⁵²

Staff agrees with SanDisk that ST contributorily infringes the '517 patent.⁴⁵³ According to Staff, the ordinary purpose of a flash memory is to be programmed and erased, which is true for flash cards, as well as USB drives.⁴⁵⁴ Therefore, Staff asserts that there are no substantial non-infringing uses and that SanDisk has met its burden of showing indirect infringement.⁴⁵⁵ In addition, Staff notes that, while ST argues that SanDisk has failed to show a specific instance of direct infringement, such infringement can be shown through circumstantial evidence.⁴⁵⁶

ST asserts that SanDisk has failed to meet its burden to prove contributory infringement because SanDisk has failed to demonstrate a specific instance of direct infringement to which ST's U.S. acts contributed and that ST's chips, standing alone, cannot infringe the '517 patent. According to ST, Dr. Rhyne conceded that there was no evidence of ST telling any manufacturer or user of a product incorporating ST's chips to issue a program command to the ST chip.⁴⁵⁷ ST also asserts that Dr. Rhyne conceded that ST's flash memory chips have substantial non-infringing uses, such as being used to store software code in consumer electronics products, such as [

] According to ST, customers load software into ST's memory during the manufacture of consumer goods outside the U.S.; therefore, there can be no infringement.⁴⁵⁸

⁴⁵² CIB 41 citing CFF 3328-41, 3343-83.

⁴⁵³ SIB 54.

⁴⁵⁴ SIB 54 citing CX-2229C (Rhyne Direct) at 387-88; Subramanian, Tr. 1370-71; Harari, Tr. 286-87.

⁴⁵⁵ SIB 54 citing *Aquatex Indus., Inc. v. Techniche Solutions*, 419 F.3d 1374, 1379, n. ** (Fed. Cir. 2005) ("*Aquatex*"); SRB 28.

⁴⁵⁶ SRB 28.

⁴⁵⁷ RIB 41 citing Rhyne, Tr. 2047-48, 2068-69; RRB 16-17.

⁴⁵⁸ RIB 42 citing Rhyne, Tr. 2055-56, 2060; [] at 110-14; [] at 107-10; *DSU Med. Corp. v. JMS Co. Ltd.*, 471 F.3d 1293, 1303-04 (Fed. Cir. 2006) ("*DSU*") (continued...)

SanDisk counters ST's arguments that SanDisk has failed to show a specific instance of direct infringement to which ST's U.S. acts contributed. According to SanDisk, the record shows that ST contributed to acts of infringement of the '517 patent in the U.S.⁴⁵⁹ SanDisk also counters ST's argument that a "read" operation constitutes a substantial non-infringing use. According to SanDisk, ST's argument ignores the fact that devices containing ST chips will be programmed in the U.S. and that the overwhelming evidence shows that an accused ST product that is in the U.S. and includes flash memory is likely to be reprogrammed in the U.S. at some point, even if it was originally programmed outside the U.S.⁴⁶⁰

ST counters SanDisk's arguments. According to ST, SanDisk's arguments merely confirm that ST's flash memories need not be reprogrammed in the U.S.; therefore, they have substantial non-infringing uses.⁴⁶¹ In addition, ST argues that SanDisk has not proven that ST knew of the '517 patent at the time when it supposedly engaged in contributory conduct. ST argues that SanDisk's mention of a parent application up the chain from the application leading the '517 patent does not show that ST knew the '517 patent existed.⁴⁶²

The undersigned finds SanDisk's and Staff's arguments persuasive. The evidence shows that the ordinary use of a flash memory involves being programmed, erased, and reprogrammed, which is true for flash memory cards and USB drives.⁴⁶³ Therefore, there are no substantial non-infringing

⁴⁵⁸(...continued)

("Section 271(c) has a territorial limitation requiring contributory acts to occur in the United States.")

⁴⁵⁹ CRB 23 citing CFF 3325-83.

⁴⁶⁰ CRB 23 citing CFF3328-41, 3343-83.

⁴⁶¹ RRB 16 citing Rhyne, Tr. 2061.

⁴⁶² RRB 17.

⁴⁶³ CX-2229C (Rhyne Direct) at 387-88; Subramanian, Tr. 1370-71; Harari, Tr. 286-87.

uses for these types of devices. Because there are no substantial non-infringing uses, SanDisk has met its burden of showing contributory infringement.

C. Domestic Industry

1. Technical Prong

SanDisk asserts that it sells a wide variety of NAND products that are protected by the '517 patent.⁴⁶⁴ According to SanDisk, its NAND products are mass storage devices and are used in a variety of applications for storing data. SanDisk asserts that its products include one or more NAND flash memory chips under the control of a controller chips and practices claims 1, 3, 5, 6, 10, and 12 of the '517 patent during programming. SanDisk also asserts that its products practice claims 7 and 8 of the '517 patent by erasing an entire block of memory cells at the same time and then programming a subset of cells within that block. The parties agree that, during normal use, SanDisk's NAND products perform program and erase operations and that SanDisk's NAND products perform these operations when SanDisk tests its products in the U.S.⁴⁶⁵ Staff agrees that, based on SanDisk's expert's testimony, SanDisk's NAND flash memory products are covered by claims 1, 3, 5, 6, 7, 8, 10, and 12 of the '517 patent.⁴⁶⁶

ST agrees that SanDisk's [] is representative of the NAND Flash chips upon which SanDisk relies to meet the domestic industry requirement for the '517 patent. In addition, ST agrees that this representative chip can operate either as a binary or MLC device.⁴⁶⁷

⁴⁶⁴ CIB 50 citing CX-902C (sample NAND products).

⁴⁶⁵ CIB 50.

⁴⁶⁶ SIB 58 citing CX-2229C (Rhyne Direct) at 313-54; SRB 30.

⁴⁶⁷ RIB 55 citing CX-2227C (Quader Direct) at A. 33, p. 7; RX-2153C (Subramanian
(continued...))

a. Claim 1

SanDisk asserts that its NAND products meet all the elements and practices all of the steps of claim 1 of the '517 patent whenever a programming operation is performed.⁴⁶⁸ As to the preamble, SanDisk asserts that there is no dispute that SanDisk's NAND products are EEPROM systems with floating gate memory cells, that the charge level of the floating gate of each cell is alterable in response to appropriate voltage conditions applied to the cell in order to set a variable threshold level, and that its products read, and determine the state of each cell.⁴⁶⁹ ST does not dispute that SanDisk's NAND products practice the preamble of claim 1 of the '517 patent.

As to the "said appropriate voltage conditions" limitation of claim 1, SanDisk asserts that there is no dispute that SanDisk's NAND products apply a series of programming pulses, in parallel, to a plurality of memory cells and that, unless a cell is inhibited, each programming pulse will alter the cell's charge level.⁴⁷⁰ ST argues that under its proposed claim construction—that claim 1 is limited to fixed pulse programming—[

]⁴⁷¹ Both SanDisk and Staff counter ST's arguments as being based on ST's faulty claim construction.⁴⁷²

The undersigned rejected ST's claim construction argument above. Therefore, ST's arguments are also rejected here and the undersigned finds that SanDisk's NAND products practice the "said appropriate voltage conditions" limitation of claim 1 of the '517 patent.

⁴⁶⁷(...continued)
Rebuttal) at A. 1857, p. 498.

⁴⁶⁸ CIB 50-53.

⁴⁶⁹ CIB 50-51.

⁴⁷⁰ CIB 51.

⁴⁷¹ RIB 55 citing RX-2153C (Subramanian Rebuttal) at A. 1893, p. 505; RRB 19-20.

⁴⁷² CRB 24; SIB 58 citing CX-2229C (Rhyne Direct) at 328; SRB 30-31.

As to the “determining” limitation of claim 1, SanDisk asserts that during program operation, SanDisk’s NAND products use a verify operation to determine, on a cell-by-cell basis, the present state of each memory cell undergoing programming. According to SanDisk, the parties agree that during the verify operation, SanDisk’s NAND products use a sense amplifier circuit to identify the present state of each cell by sensing the voltage of the cell’s bitline.⁴⁷³ SanDisk asserts that its products determine the threshold voltage range in which individual cells lie.⁴⁷⁴

ST asserts that SanDisk’s products do not perform the “determining” step because SanDisk’s NAND products [

] In other words, ST

asserts that SanDisk’s products [

]

Therefore, according to ST, SanDisk’s products do not practice the “determining” limitation for the same reason that ST’s products do not practice the “determining” limitation.⁴⁷⁵

Both SanDisk and Staff counter ST’s arguments. SanDisk counters that ST’s arguments are belied by the following facts: that the only parameter SanDisk’s NAND products intentionally alter during programming is the charge level of the cell, *i.e.* the threshold voltage; during a program-verify operation, whether or not the bitline discharges is predominantly based on the cell’s threshold voltage; and SanDisk takes manufacturing variability into account during a program-verify operation by leaving enough time for the bitline to discharge when the cell is “on,” *i.e.* erased.⁴⁷⁶

⁴⁷³ CIB 51-52.

⁴⁷⁴ CIB 52.

⁴⁷⁵ RIB 55 citing Quader, Tr. 589-90; RRB 20.

⁴⁷⁶ CRB 24.

Staff counters that SanDisk's expert testified that, in SanDisk's NAND products, the method of verifying whether the cells are programmed uses the bitline discharge method to read the cells and satisfies this limitation through determining whether the cells being read are in an erased state (in which case it conducts, or is above the threshold voltage), or in the programmed state (in which case it does not conduct).⁴⁷⁷ Staff asserts that ST's expert did not provide any testimony concerning this limitation.⁴⁷⁸ In addition, Staff asserts that, while ST contended there is manufacturing variability in the parts that allow for different results even if the cells have the same threshold voltage, SanDisk's witness testified that the key factor is the threshold voltage and that SanDisk takes manufacturing variability into account.⁴⁷⁹

ST counters SanDisk's and Staff's arguments, asserting that Dr. Quader acknowledged that

[

] ⁴⁸⁰

The undersigned finds SanDisk and Staff's arguments persuasive. While there is evidence that SanDisk's NAND products have manufacturing variability that can affect the memory state of the cells, the evidence shows that SanDisk's NAND products filter out manufacturing variability so that each cell's threshold level range is accurately determined during a program-verify operation.⁴⁸¹ Accordingly, the undersigned finds that SanDisk's NAND products practice the "determining"

⁴⁷⁷ SIB 58-59 citing CX-2229C (Rhyne Direct) at 331-38; SRB 31.

⁴⁷⁸ SIB 59 citing RX-2153C (Subramanian Rebuttal) at 504-07; Subramanian, Tr. 1374; SRB 31.

⁴⁷⁹ SIB 59 citing Quader, Tr. 581-82, 663, 695-712; SRB 31.

⁴⁸⁰ RRB 20 citing Quader, Tr. 603, 619.

⁴⁸¹ Quader, Tr. 581-82, 663, 695-712; CX-1378C (Toshiba/SanDisk NAND Flash Memory Design) at SDITC 325024.

limitation of claim 1 of the '517 patent.

As to the “terminating” limitation of claim 1, SanDisk asserts that its NAND products apply a programming pulse to a plurality of addressed memory cells in parallel, verify whether, on a cell-by-cell basis, the addressed memory cells have reached their desired states, inhibit the verified cells for the remainder of the programming operation, and continue to program, verify, and inhibit until all the plurality of addressed cells are verified.⁴⁸² ST asserts that SanDisk’s NAND products do not practice the “terminating” step because the products are subject to program disturb during which electrons can be added to the floating gate of an inhibited memory cell, thereby altering the floating gate’s charge level. Therefore, according to ST, SanDisk’s products do not practice the “terminating” limitation for the same reason that ST’s products do not practice the “terminating” limitation.⁴⁸³ Both SanDisk and Staff counter ST’s arguments as being based on ST’s faulty claim construction.⁴⁸⁴ The undersigned rejected ST’s claim construction argument for this claim limitation above. Therefore, ST’s arguments are also rejected here and the undersigned finds that SanDisk’s NAND products practice the “terminating” limitation of claim 1 of the '517 patent.

As to the final step of claim 1—the “until all plurality of cells are determined to have reached their desired threshold level ranges”—the parties agree that, during a program operation, SanDisk’s NAND products have logic that determines when all the cells in the page selected for programming are verified, ends programming based on this determination, and that once verified, each memory

⁴⁸² CIB 52.

⁴⁸³ RIB 56 citing JX-42C (Samachisa Dep) at 165-66; RX-2153C (Subramanian Rebuttal) at A. 1900, p. 506; RRB 20-21.

⁴⁸⁴ CRB 24; SIB 59-60 citing Quader, Tr. 680; CX-2229C (Rhyne Direct) at 339-41; SRB 31.

cell is permanently inhibited for the duration of the program operation.⁴⁸⁵ ST does not dispute that SanDisk's NAND products practice the "until" limitation of claim 1 of the '517 patent.

Based on the evidence above, the undersigned finds that SanDisk has proved, by a preponderance of the evidence, that its NAND products practice claim 1 of the '517 patent.

b. Dependent Claims

SanDisk asserts that ST does not dispute that SanDisk's NAND products practice the additional limitations added by claims 3, 5-8, 10, and 12 of the '517 patent.⁴⁸⁶ Specifically, SanDisk asserts that there is no dispute that SanDisk's MLC NAND memory products, which include four threshold level ranges separated by three breakpoint levels, satisfy the additional limitations of claims 3 and 5. SanDisk also asserts that there is no dispute that SanDisk's NAND products meet the additional limitations and steps of claims 7 and 8 by erasing an entire block of memory cells at the same time and then programming a subset of cells within that block. In addition, the parties agree that SanDisk's NAND products perform the program and erase operations on a single integrated circuit chip, meeting the additional limitation of claim 10. Furthermore, the parties agree that the additional limitation of claim 12 is met since, during programming, the threshold level ranges reached by SanDisk's NAND products corresponds to the chunk of input data.⁴⁸⁷

Based on the evidence above, the undersigned finds that SanDisk has proved, by a preponderance of the evidence, that its NAND products practice claims 3, 5-8, 10, and 12 of the '517 patent.

⁴⁸⁵ CIB 53.

⁴⁸⁶ CIB 53 citing ST's Pretrial Brief at 481-87; *see also* RIB 55-56 which does not include any arguments regarding the dependent claims.

⁴⁸⁷ CIB 53.

2. Economic Prong

As noted above, the undersigned issued an initial determination on November 17, 2006, granting SanDisk's motion for summary determination on domestic industry, economic prong for the '517 patent.⁴⁸⁸ On December 8, 2006, the Commission issued a notice of decision not to review the initial determination. Accordingly, no further discussion regarding the economic prong for the '517 patent is required.

D. Validity

1. Ordinary Skill in the Art

SanDisk asserts that one of ordinary skill in the art is a person with a bachelor's degree in electrical engineering, and two to three years of experience with non-volatile memory.⁴⁸⁹ ST asserts that one of ordinary skill in the art is a person with a master's degree in electrical engineering, or equivalent experience, and several years of experience in the design of floating gate memories or designing non-volatile memory circuit and systems.⁴⁹⁰ Staff asserts that one of ordinary skill in the art is a person with a master's degree in electrical engineering with several years experience in non-volatile memory design and in systems containing such memories.⁴⁹¹ According to Staff, a slightly higher level of skill in the art is appropriate with respect to the '517 patent than for the '338 patent because the '517 patent deals with systems, rather than simply a chip. Nevertheless, Staff asserts that this is not an exceptionally high or low level of skill in the art, and does not significantly affect

⁴⁸⁸ See Order No. 37 (November 17, 2006).

⁴⁸⁹ RFF 2350 citing Rao, Tr. 3181.

⁴⁹⁰ RIB 3, 61 citing Rhyne, Tr. 1726-28; RX-1801C (Subramanian Direct) at 5-6; RX-1802C (Pashley Direct) at 40.

⁴⁹¹ SIB 77 citing RX-1802C (Pashley Direct) at 40.

the analysis.⁴⁹²

The undersigned agrees with ST and Staff that a person of ordinary skill in the art to which the '517 pertains would, in 1989, have had a master's degree in electrical engineering with several years experience in the design of floating gate memories or designing non-volatile memory circuit and systems.

2. Anticipation

a. GB '145

ST asserts that U.K. patent GB 2,029,145 ("GB '145")⁴⁹³ is prior art to the '517 patent. According to ST, GB '145 discloses a permanent inhibit system to control removal of a charge from a memory cell's floating gates to avoid over erasing beyond their target state.⁴⁹⁴ Further, it discloses use of this system when adding a charge, *i.e.* programming, to cells.⁴⁹⁵ Therefore, ST asserts that GB '145 anticipates claims 1, 6, and 10 of the '517 patent.⁴⁹⁶

Specifically, ST asserts that, based on ST's and Staff's claim construction that the term "appropriate voltage conditions . . . to alter" includes both adding and removing charge from cells, there is no real dispute that GB '145 anticipates.⁴⁹⁷ ST also asserts that, as to the "ranges" limitation, SanDisk is using a different claim construction for infringement and validity, which is clearly prohibited.⁴⁹⁸

⁴⁹² SIB 77 citing 2 Donald S. Chisum, *Chisum on Patents* §§ 5.03[4][e][ii], [iii], [v] (2003) (discussing effect of different levels of skill in the art).

⁴⁹³ RX-875 (GB '145).

⁴⁹⁴ RIB 63 citing CX-2235C (Rao Direct) at A. 300, p. 85.

⁴⁹⁵ RIB 63 citing RX-875 (GB '145) at ST560-H 14151, l. 51-53).

⁴⁹⁶ RIB 63-64; RRB 23.

⁴⁹⁷ RIB 64.

⁴⁹⁸ RIB 64-65 citing *Yoon Ja Kim v. Conagra Foods, Inc.*, 465 F.3d 1312, 1324 (Fed. Cir. (continued...))

SanDisk asserts that, when claim 1 of the '517 patent is properly construed, *i.e.* only covers a program operation, not an erase operation, GB '145 does not anticipate.⁴⁹⁹ According to SanDisk, Dr. Pashley admitted that the whole purpose of GB '145 is to do erasing.⁵⁰⁰ Therefore, SanDisk asserts that GB '145 expressly teaches away from using the disclosed bitwise control of erase for a program operation.⁵⁰¹

Staff agrees with ST and asserts that the GB '145 reference anticipates claims 1, 6, and 10 (insofar as it depends from claims 1 and 6) of the '517 patent.⁵⁰² Specifically, Staff points to the testimony of ST's expert, Dr. Pashley, who testified how the GB '145 discloses all the limitations of claims 1, 6, and 10.⁵⁰³ According to Staff, SanDisk's expert, Dr. Rao, only testified that the GB '145 does not anticipate because it teaches erasing, rather than programming; therefore, it does not meet the limitations for altering the charge level and desired threshold level ranges.⁵⁰⁴ Staff notes that SanDisk's arguments are entirely based on faulty claim construction that claim 1 is limited to programming.⁵⁰⁵ In addition, Staff counters SanDisk's argument that the GB '145 reference teaches away from using programming as being irrelevant based on established case law.⁵⁰⁶

The undersigned agrees with ST and Staff that the GB '145 reference anticipates each and

⁴⁹⁸(...continued)

2006) ("*Kim*").

⁴⁹⁹ CIB 67; CRB 27.

⁵⁰⁰ CIB 67 citing CFF 4741.

⁵⁰¹ CIB 67 citing CFF4747-58.

⁵⁰² SIB 75; SRB 35-36.

⁵⁰³ SIB 75 citing RX-1802C (Pashley Direct) at 80-84.

⁵⁰⁴ SIB 75 citing CX-2235C (Rao Direct) at 210-15.

⁵⁰⁵ SIB 76.

⁵⁰⁶ SRB 36 citing *Seachange Int'l, Inc. v. C-COR Inc.*, 413 F.3d 1361, 1380 (Fed. Cir. 2005) ("*Seachange*"); *Celeritas Technologies, Ltd. v. Rockwell Int'l Corp.*, 150 F.3d 1354, 1361 (Fed. Cir. 1998), *cert. denied*, 525 U.S. 1106 (1999) ("*Celeritas*").

every limitation of claims 1, 6, and 10 of the '517 patent.⁵⁰⁷ The entirety of SanDisk's argument is based on SanDisk's claim construction that claim 1 of the '517 patent was limited to programming, which the undersigned found to be unpersuasive. Accordingly, ST has proven, by clear and convincing evidence, that claims 1, 6, and 10 of the '517 patent are anticipated by the GB '145 reference.

b. The '179 Patent

ST asserts that U.S. Patent No. 4,989,179 ("the '179 patent")⁵⁰⁸ is prior art to the '517 patent. According to ST, the '179 patent discloses a system for storing two or more bits of digital information in floating gate memory cells as multi-level digital information. Therefore, ST asserts that the '179 patent anticipates claims 1, 3, 5, 6, 10, 12, 13, and 14 of the '517 patent.⁵⁰⁹

Specifically, ST asserts that the parties dispute is narrow because Dr. Rao conceded that the '179 patent discloses the "permanent inhibit" aspect of claim 1's "terminating" limitation.⁵¹⁰ According to ST, SanDisk's and Staff's assertion that the '179 patent does not disclose the "until" limitation should be rejected, as Judge Luckern rejected a similar argument regarding claim 27 of the '338 patent.⁵¹¹ In addition, ST argues that the '179 patent also expressly teaches that the "write operation is such that the trial chargings of the column will occur until the columns are charged to a level which matches the input sample."⁵¹² According to ST, under SanDisk's claim construction of "until," the express language in the '179 patent informs a person of ordinary skill in the art how

⁵⁰⁷ RX-1802C (Pashley Direct) at 80-84.

⁵⁰⁸ CX-319/RX-712 (the '179 patent).

⁵⁰⁹ RIB 65.

⁵¹⁰ RIB 65 citing Rao, Tr. 3000.

⁵¹¹ RIB 65 citing CX-372C (the 526 ID) at 112-16; RRB 23-24.

⁵¹² RRB 23 citing CX-319/RX-712 (the '179 patent) at col. 11:57-59.

to perform the “until” method step.⁵¹³

SanDisk asserts that the ‘179 patent does not anticipate the asserted claims of the ‘517 patent because the ‘179 patent is just an analog recorder or “tape recorder on a chip.” According to SanDisk, an analog recorder programs to an exact threshold level matching the desired analog signal. Therefore, SanDisk asserts that the ‘179 patent does not disclose threshold level ranges, which is required in the “determining” and “terminating” limitations of claim 1 of the ‘517 patent.⁵¹⁴ Specifically, as to the “determining” limitation, SanDisk asserts that during programming, the comparator determines when the level in the cell matches the analog input signal to be stored and when that happens, the programming ends.⁵¹⁵ As to the “terminating” limitation, SanDisk asserts that the analog recorder applies programming conditions to each row of cells for a fixed period of time, rather than “until it is determined that all of the plurality of cells are determined to have reached their desired threshold level ranges.”⁵¹⁶

SanDisk asserts that Dr. Pashley’s testimony regarding the “digital embodiments” supposedly disclosed in the ‘179 patent is not persuasive because he is essentially rewriting the key sentence upon which he relies and because the embodiments have the same circuitry as the analog recorder and therefore operate in the same way.⁵¹⁷ SanDisk points to the testimony of Dr. Simko, who testified that prior to the 1999-2000 time frame, he had never worked on multi-level digital

⁵¹³ RRB 23-24 citing RX-1802C (Pashley Direct) at A.313; Pashley, Tr. 2478-79.

⁵¹⁴ CIB 62 citing CFF4519, 4524, 4609-12; CIB 65 citing CFF4611-16.

⁵¹⁵ CIB 65-66 citing CFF 4625-30, 4635-56; Pashley, Tr. 2556.

⁵¹⁶ CIB 66 citing CFF 4665-83; JX-43C (Simko Dep) at 76-77; CX-319/RX-712 (the ‘179 patent) at col. 11:52-56.

⁵¹⁷ CIB 62-63.

memory.⁵¹⁸

Staff asserts that the Simko '179 patent does not anticipate the asserted claims of the '517 patent because it does not satisfy the "terminating" or "until" limitations of independent claim 1.⁵¹⁹ Specifically, Staff asserts that the '179 patent applies appropriate voltage conditions for a fixed period of time and then terminates the operation regardless of whether all of the cells have reached their desired states.⁵²⁰ In addition, Staff argues that much of ST's arguments are based on Judge Luckern's anticipation and obviousness findings in the 526 investigation. Staff notes, however, that the Commission did not adopt Judge Luckern's findings on anticipation and obviousness. Therefore, Staff asserts those findings do not stand as precedent.⁵²¹

ST counters SanDisk's arguments and asserts that Dr. Pashley demonstrated two separate ways a person of ordinary skill in the art would implement the '179 patent's disclosed digital multi-level storage functionality in an EEPROM system.⁵²² First, Dr. Pashley testified about using a digital-to-analog and analog-to-digital converter. According to ST, the '179 patent discloses using an analog-to-digital converter for input and a second digital-to-analog converter for output.⁵²³ Second, Dr. Pashley testified about using discrete, repeatable tones as breakpoint threshold levels.⁵²⁴

As to whether Judge Luckern's validity findings in the 526 investigation are relevant here, the undersigned finds that because the Commission did not specifically adopt Judge Luckern's

⁵¹⁸ CIB 63 citing JX-43C (Simko Dep) at 31.

⁵¹⁹ SIB 74-75; SRB 36.

⁵²⁰ SIB 75 citing CX-2235C (Rao Direct) at 63-70, 206-08; CX-319/RX-712 (the '179 patent) at col. 11:52-56; JX-73 (Simko Dep) at 76; SRB 36.

⁵²¹ SRB 37 citing *Certain NAND Flash Memory Circuits*, Notice of Comm'n Decision at 2 (Dec. 5, 2005).

⁵²² RRB 24-25 citing Pashley, Tr. 2614-19.

⁵²³ RRB 25 citing CX-319/RX-712 (the '179 patent) at col. 4:41-45.

⁵²⁴ RRB 25 citing Pashley, Tr. 2636, 3220-21.

findings on validity, they are not determinative here. As to the substantive arguments, the undersigned finds SanDisk's and Staff's arguments regarding the "until" limitation to be persuasive. Based on the testimony presented, the '179 patent applies appropriate voltage conditions for a fixed period of time and then terminates the operation regardless of whether all of the cells have reached their desired states.⁵²⁵ Therefore, the '179 patent does not teach the "until" limitation required by claim 1 of the '517 patent. Because the '179 patent does not describe each and every element of claim 1, it does not anticipate claim 1, or any of the dependent claims of the '517 patent. Accordingly, ST has not shown, by clear and convincing evidence, that the '517 patent is invalid as anticipated by the '179 patent.

c. M293

ST asserts that the M293 is prior art to the '517 patent and anticipates claims 1, 6, and 10 of the '517 patent. According to ST, under SanDisk's claim construction, the M293 performs permanent inhibit 99.9% of the time; therefore, the M293 performs the "terminating" method step 99 out of every 100 program operations. Therefore, ST asserts that the M293 anticipates claims 1, 6, and 10 of the '517 patent.⁵²⁶

SanDisk asserts that the M293 does not anticipate the '517 patent because it performs temporary, not permanent, inhibit, which has not only been confirmed by ST's expert, Dr. Pashley, but has been found to be the case by two ALJ's and the Patent Office. In addition, the M293 is cited prior art to the '517 patent.⁵²⁷ Staff agrees with SanDisk that the M293 does not anticipate the

⁵²⁵ CX-2235C (Rao Direct) at 63-70, 206-08; CX-319/RX-712 (the '179 patent) at col. 11:52-56; JX-73 (Simko Dep) at 76; SRB 36.

⁵²⁶ RJB 67; RRB 25.

⁵²⁷ CRB 29.

asserted claims of the '517 patent because the device only uses "temporary" inhibit, a point that was conceded by ST's expert, Dr. Pashley.⁵²⁸

The undersigned finds SanDisk's and Staff's arguments to be persuasive. The evidence shows that the M293 performs temporary, rather than permanent, inhibit.⁵²⁹ In addition, the M293 was before the Patent Office during the prosecution of the '517 patent.⁵³⁰ Therefore, ST has a higher burden in showing that the M293 anticipates, which has not been shown.⁵³¹ Accordingly, ST has not shown, by clear and convincing evidence, that the '517 patent is invalid as anticipated by the M293.

3. Obviousness

ST asserts that the asserted claims of the '517 patent are obvious over either the Japanese Unexamined Patent Application S62-188100 ("JP100")⁵³² reference standing alone or in combination with other references.⁵³³ Staff agrees that the asserted claims are rendered obvious by JP100 in combination with the '179 patent and/or the '344 patent.⁵³⁴ SanDisk counters, arguing that there is a lack of motivation to combine.⁵³⁵

The undersigned notes that all of the parties post-hearing briefs and reply briefs were filed before the Supreme Court issued its decision in *KSR*.⁵³⁶ On May 25, 2007, counsel from SanDisk and ST submitted a letter to the undersigned requesting guidance whether the undersigned would find

⁵²⁸ SRB citing RX-1802C (Pashley Direct) at 85.

⁵²⁹ RX-1802C (Pashley Direct) at 85.

⁵³⁰ See CX-99/RX-2 (the '517 patent), first page.

⁵³¹ *Liebel-Flarsheim Co. v. Medrad, Inc.*, 481 F.3d 1371, 1381 (Fed. Cir. 2007) ("*Liebel-Flarsheim II*") citing *Glaxo*, 376 F.3d at 1348 (burden of showing invalidity is "especially difficult" when the prior art reference was before the examiner during prosecution).

⁵³² RX-800 (JP100).

⁵³³ RIB 67.

⁵³⁴ SIB 77-82; SRB 37-40.

⁵³⁵ CIB 72-83; CRB 29-38.

⁵³⁶ *KSR*, *supra*.

additional briefing useful in light of *KSR*. SanDisk's position is that additional briefing would be useful to several of the factual inquiries required in the obviousness analysis, while ST's position is that *KSR*'s affect on the parties existing § 103 arguments is clear. Staff does not object to additional briefing if the undersigned would find such briefing useful. In reviewing the Supreme Court's decision and the evidence and briefing on the obviousness issues, the undersigned had already determined that additional briefing would neither be helpful nor necessary. Nothing in the joint letter has changed this determination. Accordingly, no additional briefing will be required on obviousness.

Upon review of the parties arguments, the undersigned finds that much of the dispute between the parties is whether ST has made an adequate showing of a motivation to combine the various prior art references. While the Supreme Court, in *KSR*, noted that there is "no necessary inconsistency between the idea underlying the TSM [teaching, suggestion, or motivation] test and the *Graham* analysis," the Supreme Court made it clear that the TSM test was being applied too rigidly and against prior Supreme Court precedents:

In determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose of the patentee controls. What matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid under § 103. One of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims.

The first error of the Court of Appeals in this case was to foreclose this reasoning by holding that courts and patent examiners should look only to the problem the patentee was trying to solve. . . . The Court of Appeals failed to recognize that the problem motivating the patentee may be only one of many addressed by the patent's subject matter. The question is not whether the combination was obvious to the patentee but whether the combination was obvious to a person with ordinary skill in the art. Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

The second error of the Court of Appeals lay in its assumption that a person of ordinary skill attempting to solve a problem will be led only to those elements of prior art designed to solve the same problem. . . . Common sense teaches, however, that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. . . . A person of ordinary skill is also a person of ordinary creativity, not an automaton.

The same constricted analysis led the Court of Appeals to conclude, in error, that a patent claim cannot be proved obvious merely by showing that the combination of elements was "obvious to try." *Id.*, at 289 (internal quotation marks omitted). When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under § 103.

The Court of Appeals, finally, drew the wrong conclusion from the risk of courts and patent examiners falling prey to hindsight bias. A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning. See *Graham*, 383 U.S., at 36, 86 S. Ct. 684, 15 L. Ed. 2d 545 (warning against a "temptation to read into the prior art the teachings of the invention in issue" and instructing courts to "'guard against slipping into the use of hindsight'" (quoting *Monroe Auto Equipment Co. v. Heckethorn Mfg. & Supply Co.*, 332 F.2d 406, 412 (CA6 1964))). Rigid preventative rules that deny factfinders recourse to common sense, however, are neither necessary under our case law nor consistent with it.⁵³⁷

Based on a reading of the Supreme Court's precedent in *KSR*, the undersigned finds that many of the parties' specific "motivation to combine" arguments fall within the scope of what the Supreme Court has cautioned as being applied too rigidly. Therefore, the undersigned will focus on the original *Graham* factors to determine whether the '517 patent is obvious under § 103.

a. JP100

ST asserts that JP100, when modified as known to those of skill in the art, renders claims 1,

⁵³⁷ *KSR*, 500 U.S. at – ; 127 S.Ct. at 1741-43.

6, and 10 of the '517 patent obvious.⁵³⁸ ST asserts that SanDisk's conceded that the only limitation of claim 1 that is not disclosed by JP100 is an electrical erase capability.⁵³⁹ According to ST, one of skill in the art would have been motivated to modify JP100 to include the electrical erase capability for numerous reasons.⁵⁴⁰

SanDisk asserts that the '517 patent is directed to "semiconductor electrically erasable programmable read-only memories (EEPROM), and specifically to a system of integrated circuit Flash EEPROM chips,"⁵⁴¹ while JP100 is directed to a completely different "field of endeavor."⁵⁴² According to SanDisk, the purpose of JP100 was to obtain a writing method fitted for pre-processing of a storage characteristic test, sometimes referred to as a memory maintenance characteristic test.⁵⁴³ According to SanDisk, in 1989, a person of ordinary skill in the art faced with the problems that were faced by the inventors of the '517 patent would have no reason to select elements from JP100 and combine it with missing elements to obtain the claimed invention.⁵⁴⁴

SanDisk also asserts that JP100 does not disclose any "programming methods" for an EPROM. While SanDisk concedes that JP100 repeatedly makes reference to a method of writing to EPROMs, it does not ever make reference to a method of programming EPROMs.⁵⁴⁵ As to ST's assertion that JP100 teaches a way to avoid over-programming, SanDisk asserts that JP100 avoids over-programming for completely different reasons than in the '517 patent. According to SanDisk, the

⁵³⁸ RIB 68 citing *Sibia Neurosciences, Inc. v. Cadus Pharm. Corp.*, 225 F.3d 1349, 1356 (Fed. Cir. 2000) ("*Sibia*").

⁵³⁹ RIB 68 citing Complainant's prehearing brief at 455; Rao, Tr. 3009-10.

⁵⁴⁰ RIB 68 citing RX-1802C (Pashley Direct) at A. 224, p. 54.

⁵⁴¹ CRB 31 citing CX-99/RX-2 (the '517 patent) at col. 1:25-28.

⁵⁴² CRB 31 citing *Wang Laboratories, supra*.

⁵⁴³ CIB 79 citing CX-1247 (JP100 abstract); RX-800 (JP100) at ST560-H 19203.

⁵⁴⁴ CIB 79, 82.

⁵⁴⁵ CIB 80 citing RX-800 (JP100) at ST560-H19203.

inventors in the '517 patent used permanent inhibit to prevent over-programming, while JP100 seeks to avoid over-programming to align to a specific level the threshold voltage as a starting point for data retention testing.⁵⁴⁶ In addition, SanDisk asserts that over-programming is not the problem that the inventors of the '517 patent were seeking to solve; rather, it was an aspect of their solution.⁵⁴⁷ Therefore, SanDisk asserts that ST is improperly attempting to define the problem in terms of its solution, based on hindsight.⁵⁴⁸

SanDisk counters ST's four motivations for modifying JP100 to obtain the claimed invention of claim 1 of the '517 patent. SanDisk asserts that ST's first two motivations ignore any motivation to select JP100 to solve the problem faced by the inventors of the '517 patent and merely asserts that adding such erase capability is desirable. SanDisk asserts that ST's third motivation, *i.e.* improvements the JP100 made to reliability testing, has nothing to do with the problem faced by the inventors. SanDisk asserts that ST's fourth motivation, *i.e.* that an enhanced write operation for EEproms and Eproms that minimizes stress to the device is one of the stated objects of the '517 invention, misrepresents the '517 patent because the '517 patent never mentions Eproms, only Flash EEproms.⁵⁴⁹

Staff does not take a position on the JP100 reference standing alone, only in combination with other references, which is discussed below.

The undersigned rejects SanDisk's arguments, as they are based on the rigid "motivation to combine" framework that has been rejected by the Supreme Court in *KSR*. The undersigned also

⁵⁴⁶ CIB 81 citing RX-800 (JP100) at ST560-H19203.

⁵⁴⁷ CIB 81-82.

⁵⁴⁸ CIB 82 citing *Monarch Knitting Mach. Corp. v. Sulzer Morat GMBH*, 139 F.2d 877, 881 (Fed. Cir. 1998) ("*Monarch*").

⁵⁴⁹ CRB 33 citing CX-99/RX-2 (the '517 patent) at col. 1:41-60.

finds ST's argument persuasive. SanDisk's expert, Dr. Rao, conceded that JP100 disclosed every element of claim 1 except for the first "E" in EEprom:

- Q. Indeed, you would agree with me that the JP-100 shows all of the elements of claim 1 of the '517 except that it is an EPROM instead of an EEPROM?
- A. Can I look at the claim 1 of '517? Quickly. Quickly. It won't take --
- Q. It's RX-2. We can pull it up -- can you put claim 1 on the screen, please.
- A. That will be fine.
- Q. There it is.
- A. Yes. I agree with that.⁵⁵⁰

At the time of the '517 patent, one of ordinary skill would recognize that adding an erase electrode to make an Eprom into an EEprom would be advantageous.⁵⁵¹ Therefore, the suggestion to make such a modification is in the prior art itself and is part of the knowledge of one of ordinary skill in the art. The undersigned finds that for a person of ordinary skill in the art in the non-volatile memory field, that person would naturally look to Eprom solutions in the development of EEproms.⁵⁵² Accordingly, ST has shown, by clear and convincing evidence, that claim 1 of the '517 patent is invalid as obvious based on the JP100 reference.⁵⁵³

⁵⁵⁰ Rao, Tr. 3009-10.

⁵⁵¹ RX-1802C (Pashley Direct) at A. 224-32, 236-53, 258-58.

⁵⁵² See *Para-Ordnance Mfg., Inc. v. SGS Importers Int'l, Inc.*, 73 F.3d 1085, 1090 (Fed. Cir. 1995) ("*Para-Ordnance*"); *In re Gartside*, 203 F.3d 1305, 1321 (Fed. Cir. 2000) ("*Gartside*").

⁵⁵³ *In re Kotzab*, 217 F.3d 1365, 1370 (Fed. Cir. 2000) ("*Kotzab*") ("The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved. See [*In re*] *Dembiczak*, 175 F.3d [994] at 999, 50 USPQ2d at 1617 [Fed. Cir. 1999]. In addition, the teaching, motivation or suggestion may be implicit from the prior art as a whole, rather than expressly stated in the references. See *WMS Gaming, Inc. v. International Game Tech.*, 184 F.3d 1339, 1355, 51 USPQ2d 1385, 1397 (Fed. Cir. 1999). The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 881 (1981) (and cases cited therein). Whether the Board relies on an express or an implicit showing, it must provide particular findings related thereto. See *Dembiczak*, 175 F.3d at 999, 50 USPQ2d at 1617. Broad conclusory statements standing alone are not 'evidence.' *Id.*")

b. JP100 and the '179 Patent

ST asserts that JP100, when combined with the '179 patent, renders claims 1, 3, 5, 6, 7, 10, 12, 13, and 14 of the '517 patent obvious.⁵⁵⁴ ST asserts that SanDisk's expert conceded that the only limitations of these claims that are missing from the '179 patent, *i.e.* the presence of threshold level ranges and the "until" limitation, are found in JP100.⁵⁵⁵ According to ST, one of skill in the art would have been motivated to combine JP100 and the '179 patent for numerous reasons.⁵⁵⁶

Specifically, ST asserts that the motivation to combine lies in the nature of the problem addressed by the invention, *i.e.* how to prevent over-programming of memory cells. According to ST, both JP100 and the '179 patent directly address the problem and teach permanent inhibit to solve it.⁵⁵⁷ Therefore, ST asserts that to a person of ordinary skill in the art working on the problem of preventing over-programming of a memory cell, it would have been obvious to bring together the method and structure of permanently inhibiting shown in JP100 and the '179 patent to arrive at the claimed invention in the '517 patent.⁵⁵⁸ ST also asserts that a motivation to combine can be found in the patents' cross-referential teaching on testing.⁵⁵⁹

SanDisk asserts that, in 1989, a person of ordinary skill in the art that was faced with the problems that were faced by the inventors of the '517 patent would have no reason to select elements from the '179 patent and combine it with missing elements to obtain the claimed invention.

⁵⁵⁴ RIB 69 citing RX-1802C (Pashley Direct) at A. 853-903, p. 204-15.

⁵⁵⁵ RIB 69.

⁵⁵⁶ RIB 69 citing RX-1802C (Pashley Direct) at A. 686-88, p. 166; A. 874-76, p. 209-10; A. 900, p. 215.

⁵⁵⁷ RRB 33 citing *Sibia*, 225 F.3d at 1356; RX-800 (JP100) at ST560-H 19203-04; CX-319/RX-712 (the '179 patent) at col. 10:47-53.

⁵⁵⁸ RRB 33 citing *Ruiz v. A.B. Chance Co.*, 357 F.3d 1270, 1276 (Fed. Cir. 2004) ("*Ruiz*").

⁵⁵⁹ RRB 33.

Specifically, SanDisk asserts that the Simko invention is merely a “tape recorder on a chip” addressing the problem with digital recorders that has nothing to do with the problem to be solved by the ‘517 patent, which is to providing solid-state mass storage for computer systems. SanDisk points to the testimony of Dr. Simko, who stated that the analog recorder required “reasonable” precision, and could therefore tolerate small errors, whereas Flash EEPROMs suitable for computer mass storage require a high level of precision. SanDisk also argues that the Simko analog recorder operated at a low speed when compared with a high-performance EEPROM.⁵⁶⁰ SanDisk asserts that the ‘179 patent does not disclose any digital embodiments,⁵⁶¹ and that the comparator in the ‘179 patent cannot determine a cell’s threshold level range because it can only determine its threshold level.⁵⁶² As to claim 7, SanDisk asserts that ST failed to raise this issue in its pretrial brief; therefore the issue is waived under Ground Rule 8.2. Furthermore, SanDisk asserts that Dr. Pashley did not testify that JP100 in combination with the ‘179 patent renders claim 7 obvious.⁵⁶³

ST counters SanDisk’s arguments that these two pieces of prior art are not analogous because both of them are not directed to replacing “mass storage” in computers. ST argues that, based on the clear motivations to combine, the argument is irrelevant.⁵⁶⁴

Staff asserts that claims 1, 3, 5, 6, 10, 12, 13, and 14 of the ‘517 patent are invalid under 35 U.S.C. § 103(a) in view of JP100 in combination with the ‘179 patent.⁵⁶⁵ Specifically, Staff points to the testimony of ST’s expert, Dr. Pashley, who testified how each of the limitations of the

⁵⁶⁰ CIB 77 citing CFF 5368-77; CX-319/RX-712 (the ‘179 patent) at col. 1:36-39, 6:20-29.

⁵⁶¹ CIB 78 citing CFF 4589-90, 4593.

⁵⁶² CRB 37 citing CFF 4628-30.

⁵⁶³ CRB 36.

⁵⁶⁴ RRB 33-34.

⁵⁶⁵ SIB 77-78; SRB 37.

asserted claims is satisfied by JP100 in combination with the '179 patent.⁵⁶⁶ According to Staff, as to claim 1 of the '517 patent, while SanDisk's expert, Dr. Rao, argues that the limitations that were not taught by the '179 patent include "a variable threshold level of a cell" that is "set into range determinable by reading a cell"; "determining the threshold level ranges"; and continuing the programming, verifying and inhibiting processes "until all of the plurality of cells are determined to have reached their desired threshold level ranges," Dr. Rao acknowledges that all of these limitations are taught by JP100.⁵⁶⁷ As to claims 6 and 10, Staff asserts that Dr. Rao did not dispute that the '179 patent teaches these additional limitation.⁵⁶⁸ As to claims 3 and 5, Staff asserts that while Dr. Rao testified that the '179 patent does not disclose the multiple threshold ranges limitations, clear and convincing evidence shows that the '179 patent does disclose such ranges.⁵⁶⁹ As to claims 12, 13, and 14, Staff asserts that while Dr. Rao testified that the '179 patent does not teach the "chunk of input data" or "cache memory" limitations, clear and convincing evidence shows that the '179 patent does disclose limitations.⁵⁷⁰ In addition, Staff asserts that ST has made a clear and convincing showing of motivation to combine. According to Staff, ST's expert testified that a person of ordinary skill in the art would be motivated to combine the references in order to made a superior EEprom, which is confirmed by the references themselves, *i.e.* the '179 patent teaches a floating gate EEprom, while JP100 relates to improving methods of writing to floating gate Eproms.⁵⁷¹

Staff argues that SanDisk does not appear to seriously contest that this combination discloses

⁵⁶⁶ SIB 78 citing RX-1802C (Pashley Direct) at 204-15.

⁵⁶⁷ SIB 78 citing CX-2235C (Rao Direct) at 216-17.

⁵⁶⁸ SIB 78 citing CX-2235C (Rao Direct) at 216.

⁵⁶⁹ SIB 78 citing CX-2235C (Rao Direct) at 219 and RX-1802C (Pashley Direct) at 210-12.

⁵⁷⁰ SIB 78 citing CX-2235C (Rao Direct) at 216 and RX-1802C (Pashley Direct) at 214.

⁵⁷¹ SIB 79 citing RX-1802C (Pashley Direct) at 208-10, 215; CX-319/RX-712 (the '179 patent) at col. 1:56-2:25, 3:10-12; RX-800 (JP100) at 19201.

all of the limitations of the asserted claims. Rather, Staff notes that SanDisk appears to rely on the alleged lack of motivation to combine.⁵⁷² In Staff's view, both JP100 and the '179 patent are directed to the same problem addressed in the '517 patent, which is how to improve programming techniques for floating gate memory cells.⁵⁷³

The undersigned rejects SanDisk's arguments, as they are based on the rigid "motivation to combine" framework that has been rejected by the Supreme Court in *KSR*. The undersigned also agrees with ST and Staff that the evidence shows that claims 1, 3, 5, 6, 10, 12, 13, and 14 of the '517 patent are taught by JP100 in combination with the '179 patent.⁵⁷⁴ The undersigned agrees that SanDisk did not seriously contest that this combination discloses all of the limitations of the asserted claims and relies primarily on its "motivation to combine" arguments, which have been rejected. The undersigned finds that the references are closely related, as the JP100 reference relates to improving methods of writing to floating gate Eproms, while the '179 patent relates to floating gate EEproms. According to the '338 patent, which is incorporated by reference into the '517 patent, the problems of improving Eproms and EEproms are closely related.⁵⁷⁵ Therefore, it would be reasonable for a person of ordinary skill in the non-volatile memory field to naturally look to Eprom solutions in the development of EEproms and combine the references together.

As for claim 7, the undersigned finds SanDisk's procedural argument to be persuasive. A review of ST's pre-trial brief shows no mention of ST's intention to argue that JP100 in combination

⁵⁷² SRB 37.

⁵⁷³ SRB 37-38 citing CX-99/RX-2 (the '517 patent) at col. 1:59-60; RX-800 (JP100) at 19200; CX-319/RX-712 (the '179 patent) at col. 2:43-46.

⁵⁷⁴ See RX-1802C (Pashley Direct) at 204-15.

⁵⁷⁵ See CX-99/RX-2 (the '517 patent) at col. 8:30-37; CX-98/RX-1 (the '338 patent) at col. 2:23-25, 2:30-33.

with the '179 patent renders claim 7 of the '517 patent obvious.⁵⁷⁶ Therefore, ST's assertion that claim 7 of the '517 patent is obvious based on JP100 in combination with the '179 patent is rejected.

Accordingly, ST has shown, by clear and convincing evidence, that claims 1, 3, 5, 6, 10, 12, 13, and 14 of the '517 patent are invalid as obvious based on the JP100 reference in combination with the '179 patent. Claim 7 of the '517 patent, however, is not found to be invalid as obvious based on the JP100 reference in combination with the '179 patent.

c. JP100 and the '344 patent

ST asserts that JP100, when combined with U.S. Patent No. 5,095,344 ("the '344 patent"),⁵⁷⁷ renders claims 1, 3, 5, 6, 7, 8, 10, 12, 13, and 14 of the '517 patent obvious.⁵⁷⁸ According to ST, the '344 patent is directed to increasing the amount of information stored in an Eeprom or EEprom array of a given size and providing EEprom semiconductor chips to be used for solid state memory to replace magnetic storage devices.⁵⁷⁹ ST asserts that one of ordinary skill in the art would have been motivated to combine JP100 and the '344 patent for numerous reasons.⁵⁸⁰ Specifically, ST asserts that there is a motivation stemming from technological progress and that the references themselves practically cross-reference each other.⁵⁸¹

Specifically, ST asserts that the '344 patent discloses multilevel programming of EEprom cells using more than two threshold levels separated by more than one breakpoint threshold level

⁵⁷⁶ See ST's pretrial brief at 565.

⁵⁷⁷ RX-362 (the '344 patent).

⁵⁷⁸ RIB 69-70 citing RX-1802C (Pashley Direct) at A. 193-208, 383-91, 904-33.

⁵⁷⁹ RIB 70 citing RX-362 (the '344 patent) at col. 2:33-36.

⁵⁸⁰ RIB 70-72.

⁵⁸¹ RIB 70; RRB 34 citing RX-1802C (Pashley Direct) at A. 236-53.

range.⁵⁸² ST argues that SanDisk's expert, Dr. Rao, conceded that the '344 patent discloses the multi-state elements of the '517 claims 3 and 5 that were missing from JP100.⁵⁸³ According to ST, a person of ordinary skill in the art would have been motivated to modify the structure disclosed in JP100 with an erasable, multilevel structure of the '344 patent in order to make a more compact EEPROM. In addition, ST asserts that it was common knowledge in the EEPROM art that higher integration or density is and always has been a basic goal of memory design.⁵⁸⁴

As to claims 7, 8, and 10, ST asserts that JP100, in combination with the '344 patent, discloses these additional limitations. According to ST, the limitations of claims 7 and 8 were known to those of ordinary skill in the art.⁵⁸⁵ ST argues that a person of ordinary skill in the art modifying JP100 to include erase capability in light of the '344 patent would be aware of the benefits of the different units of erase, including blocks, sectors, and wordlines.⁵⁸⁶

As to claims 12, 13, and 14, ST asserts that the only limitations Dr. Rao does not concede to be disclosed by JP100 in combination with the '344 patent are the "chunk of input data" in claims 12 and 13, and the "cache memory" in claim 14.⁵⁸⁷ According to ST, a person of ordinary skill in the art that was combining JP100 and the '344 patent would use data latches for storing input data on a chip during an internally timed write cycles, which would meet the additional limitations in claims

⁵⁸² RIB 70 citing RX-362 (the '344 patent) at col. 24:5-38.

⁵⁸³ RIB 70 citing CX-2235C (Rao Direct) at A. 874, p. 221.

⁵⁸⁴ RIB 70 citing RX-1802C (Pashley Direct) at A. 912, p. 218-19; A. 243, p. 57.

⁵⁸⁵ RIB 70-71 citing CX-2235C (Rao Direct) at A. 1026, p. 261; JX-38C (Mehrotra Dep) at 126-128; RX-889 (SEEQ 48F512 datasheet) at SDITC-II 7043-44; CX-99/RX-2 (the '512 patent) at col. 7:6-13.

⁵⁸⁶ RIB 71 citing RX-1802C (Pashley Direct) at A. 108-13, p. 29-30.

⁵⁸⁷ RIB 70 citing Rao, Tr. 3139; CX-2235C (Rao Direct) at A. 874-75, p. 221.

12-14.⁵⁸⁸

SanDisk does not address this combination in its post-trial brief, but does address this combination in its post-trial reply brief.⁵⁸⁹ ST asserts that, because SanDisk failed to raise this issue in its post-trial brief, under Ground Rule 11.1, SanDisk has waived its ability to do.⁵⁹⁰

Staff agrees that claims 1, 3, 5, 6, 7, 8, and 10 of the '517 patent are invalid under 35 U.S.C. § 103(a) in view of JP100 in combination with the '344 patent.⁵⁹¹ Specifically, Staff points to the testimony of ST's expert, Dr. Pashley, who testified how each of the limitations of the asserted claims is satisfied by JP100 in combination with the '344 patent.⁵⁹² Staff argues that SanDisk does not appear to seriously contest that this combination discloses all of the limitations of the asserted claims. Rather, Staff notes that SanDisk appears to rely on the alleged lack of motivation to combine.⁵⁹³ According to Staff, ST's expert testified that a motivation to combine exists both in the nature of the problem to be solved and in the explicit disclosure of the '344 patent that it would be desirable to convert an Eprom into an EEprom.⁵⁹⁴

As to the procedural issue, the undersigned agrees that SanDisk did not address the '344 patent at all in its obviousness section in its post-hearing brief, and that SanDisk has waived any arguments with regard to this combination.⁵⁹⁵ ST clearly briefed this issue extensively in its pre-trial

⁵⁸⁸ RIB 71 citing Pashley, Tr. 2644, 2848-51; RX-947 (JEDEC Standard 21-B) at ST560 461384, 461396; RX-1802C (Pashley Direct) at A. 98-103, p. 26-27. A. 279-91, p. 68-71.

⁵⁸⁹ CRB 33-36.

⁵⁹⁰ RRB 34.

⁵⁹¹ SIB 80; SRB 37.

⁵⁹² SIB 80 citing RX-1802C (Pashley Direct) at 216-21.

⁵⁹³ SIB 80; SRB 37 citing CX-2235C (Rao Direct) at 221.

⁵⁹⁴ SIB 80 citing RX-1802C (Pashley Direct) at 216, 222-23).

⁵⁹⁵ See Order No. 2 (February 14, 2006), Ground Rule 11.1.

brief⁵⁹⁶ and this obviousness combination was discussed in detail during the hearing.⁵⁹⁷ Therefore, SanDisk should have known that ST was going to advance this obviousness combination in the post-trial briefs and SanDisk should have addressed its arguments in the post-trial brief.

The undersigned agrees with ST and Staff that the evidence shows that all the limitations of claims 1, 3, 5, 6, 7, 8, and 10 of the '517 patent are taught by JP100 in combination with the '344 patent.⁵⁹⁸ The undersigned finds that the references are closely related, as the JP100 reference relates to improving methods of writing to floating gate Eproms by aligning to a reference cell and using permanent inhibit, while the '344 patent relates to an intelligent programming and sensing technique to allow for practical implementation of multistate storage.⁵⁹⁹ Accordingly, ST has shown, by clear and convincing evidence, that all of the asserted claims of the '517 patent are invalid as obvious based on the JP100 reference in combination with the '344 patent.

d. JP100 and the '871 patent

ST asserts that JP100, when combined with U.S. Patent No. 4,752,871 ("the '871 patent"),⁶⁰⁰ renders claims 1, 6, 7, 8, 10, 12, 13, and 14 of the '517 patent obvious.⁶⁰¹ According to ST, one of ordinary skill in the art would have been motivated to combine JP100 and the '871 patent for numerous reasons, including making testing process improvements.⁶⁰² As for the additional limitations in claims 7 and 8, ST asserts that a person of ordinary skill in the art would be highly

⁵⁹⁶ See ST's pre-trial brief at 582.

⁵⁹⁷ See, generally, the testimony of Dr. Pashley and Dr. Rao, Tr. 2720-22, 2763-64, 2861-64, 2873-76, 3138-41.

⁵⁹⁸ See RX-1802C (Pashley Direct) at 216-21.

⁵⁹⁹ See RX-800 (JP100) at 19203-06; RX-362 (the '344 patent) at col. 3:24-29.

⁶⁰⁰ RX-351 (the '871 patent).

⁶⁰¹ RIB 72 citing RX-1802C (Pashley Direct) at A. 193-206, 372-76, 934-64.

⁶⁰² RIB 72 citing RX-1802C (Pashley Direct) at A. 944, p. 225-26.

motivated to combine the block erasable, byte programmable architecture of the '871 patent because it increases the speed of testing with the permanent inhibit circuitry that increases the accuracy of programming in testing.⁶⁰³

SanDisk asserts that the '871 patent has nothing to do with the problem of developing EEproms to replace computer disk drives; therefore there would be no reason for a person of ordinary skill in the art, faced with the problem of developing EEproms to replace computer disk drives, would select the '871 patent. In addition, SanDisk asserts that the '871 patent does not disclose block erase, which is required by claims 7 and 8.⁶⁰⁴

Staff asserts that ST has failed to show, by clear and convincing evidence, that the asserted claims of the '517 patent are invalid under 35 U.S.C. § 103(a) in view of JP100 in combination with the '871 patent.⁶⁰⁵ According to Staff, the '871 patent discloses a microcomputer that uses on-chip EEprom arrays, which is a different technique than used in JP100.⁶⁰⁶ Staff asserts that ST's expert, Dr. Pashley, merely testified that one would want to divide JP100 into multiple arrays without testifying whether the system of the '871 patent would work in doing so.⁶⁰⁷

The undersigned agrees with SanDisk and Staff that ST has failed to show, by clear and convincing evidence, that the asserted claims of the '517 patent are invalid as obvious based on JP100 in combination with the '871 patent because ST did not provide adequate evidence on how the two references can combine the missing elements to obtain the claimed invention in the '517

⁶⁰³ RRB 36-37 citing RX-1802C (Pashley Direct) at A. 944.

⁶⁰⁴ CRB 38 citing CFF 5538-5855.

⁶⁰⁵ SIB 81; SRB 39, n. 6.

⁶⁰⁶ SIB 81 citing RX-351 (the '871 patent), Fig. 1; CX-2235C (Rao Direct) at 98-100.

⁶⁰⁷ SIB 81 citing RX-1802C (Pashley Direct) at 227.

patent.⁶⁰⁸ Accordingly, ST has failed to show, by clear and convincing evidence, that the '517 patent is invalid as obvious based on JP100 in combination with the '871 patent.

e. JP 100 and the '541 patent

ST asserts that JP100, when combined with U.S. Patent No. 5,136,541 ("the '541 patent"),⁶⁰⁹ renders claims 1, 6, 7, 8, 10, 12, 13, and 14 of the '517 patent obvious.⁶¹⁰ According to ST, one of ordinary skill in the art would have been motivated to combine JP100 and the '541 patent for numerous reasons, including the references pointing to one another.⁶¹¹ ST counters Staff's argument that the '541 is different from JP100. According to ST, the '541 patent provides electrical erase to JP100's permanent inhibit.⁶¹²

SanDisk asserts that the '541 patent has nothing to do with the problem of developing EEproms to replace computer disk drives; therefore there would be no reason for a person of ordinary skill in the art, faced with the problem of developing EEproms to replace computer disk drives, to select the '541 patent. In addition, SanDisk asserts that the '541 patent does not disclose block erase, which is required by claims 7 and 8.⁶¹³

Staff asserts that ST has failed to show, by clear and convincing evidence, that the asserted claims of the '517 patent are invalid under 35 U.S.C. § 103(a) in view of JP100 in combination with the '541 patent.⁶¹⁴ According to Staff, the '541 patent erases by injecting holes, which is a

⁶⁰⁸ CX-2235C (Rao Direct) at 98-100; RX-1802C (Pashley Direct) at 227.

⁶⁰⁹ RX-25 (the '541 patent).

⁶¹⁰ RIB 72 citing RX-1802C (Pashley Direct) at A. 193-206, 372-76, 934-64.

⁶¹¹ RIB 73 citing RX-1802C (Pashley Direct) at A. 243, p. 57; RRB 36.

⁶¹² RRB 36 citing *Amgen*, 314 F.3d at 1357.

⁶¹³ CRB 38 citing CFF 5538-5855.

⁶¹⁴ SIB 81; SRB 39, n. 6.

different technique than used in JP100.⁶¹⁵ Staff asserts that ST's expert, Dr. Pashley, merely testified as to block erase without discussing how or why the '541 patent would be combined with JP100 to provide for block erase.⁶¹⁶

The undersigned agrees with SanDisk and Staff that ST has failed to show, by clear and convincing evidence, that the asserted claims of the '517 patent are invalid as obvious based on JP100 in combination with the '541 patent because ST did not provide adequate evidence on how the two references can combine the missing elements to obtain the claimed invention in the '517 patent.⁶¹⁷ Accordingly, ST has failed to show, by clear and convincing evidence, that the '517 patent is invalid as obvious based on JP100 in combination with the '541 patent.

f. Secondary Considerations

SanDisk asserts that secondary indicia of non-obviousness such as long felt need coupled with failure of others, commercial success, and industry praise supports the validity of the '517 patent.⁶¹⁸ According to SanDisk, at the time of the invention of the '517 patent, there was a long-felt need in the industry for the invention of the '517 patent, *i.e.* a memory device that provided the advantages of a magnetic memory device while avoiding its limitations. SanDisk asserts that while many others developed competing devices which failed, the inventors of the '517 patent succeeded.⁶¹⁹ SanDisk also points to the commercial success of both SanDisk's and Toshiba's

⁶¹⁵ SIB 81 citing RX-25 (the '541 patent) at col. 3:21-24; CX-2235C (Rao Direct) at 94-95.

⁶¹⁶ SIB 81 citing RX-1802C (Pashley Direct) at 233.

⁶¹⁷ CX-2235C (Rao Direct) at 94-95; RX-1802C (Pashley Direct) at 233.

⁶¹⁸ CIB 83 citing *Intel Corp. v. U.S. Int'l Trade Comm'n*, 946 F.2d 821, 835 (Fed. Cir. 1991) ("*Intel*"); CRB 38.

⁶¹⁹ CIB 83 citing CFF6769-6817.

NAND flash memory products, both of which practice the '517 patent.⁶²⁰ In addition, SanDisk asserts that it has won industry accolades and awards for its NAND flash memory products.⁶²¹

ST asserts that SanDisk's arguments regarding secondary considerations are not supported by the evidence. Furthermore, ST asserts that where there is a strong motivation to combine, secondary considerations cannot save the claims.⁶²² Specifically, as to lack of commercial success, ST asserts that SanDisk has failed to prove any commercial success that is owed to the point of novelty in the '517 patent, *i.e.* "permanent inhibit."⁶²³ According to ST, for several years after the invention, SanDisk's products [

] ⁶²⁴ As for SanDisk's NOR products, initially, [

] ⁶²⁵ In addition, ST argues that the success of SanDisk's NAND market stems from Toshiba, [

] ⁶²⁶ And while SanDisk relies on licensing to demonstrate its commercial success, ST asserts that SanDisk has failed to show sufficient nexus between the licenses and the patent at issue.⁶²⁷

ST asserts that the '179 patent, JP100, and GB '145 all had permanent inhibit prior to the date of the invention of the '517 patent and that Texas Instruments was working on permanent inhibit in 1985-86.⁶²⁸ Therefore, ST asserts that the concept that SanDisk touted as the novel feature

⁶²⁰ CIB 83 citing CFF6818-44.

⁶²¹ CIB 83-84 citing CFF6845-55.

⁶²² RIB 78-79 citing *Sibia*, 225 F.3d at 1358.

⁶²³ RIB 79; RRB 38.

⁶²⁴ RRB 38 citing Harari, Tr. 354.

⁶²⁵ RIB 79 citing Harari, Tr. 354; JX-36C (Harari Dep) at 174.

⁶²⁶ RRB 38 citing *In re Huang*, 100 F.3d 135, 140 (Fed. Cir. 1996) ("*Huang*").

⁶²⁷ RIB 79; RRB 38 citing *Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1324 (Fed. Cir. 2004) ("*Iron Grip*"); *GPAC.*, *supra*; *Sibia*, 225 F.3d at 1358.

⁶²⁸ RIB 79 citing Rao, Tr. 3000, 3008, 3014, 3081.

during the '517 patent prosecution was already known in the programming, erasing, and testing context before the date of invention.⁶²⁹

As to failure by others, ST asserts that there is none. According to ST, a paper describing the device embodying the prior art permanent inhibit of the '179 patent technology was published in a prestigious engineering journal and the product commercializing the '179 patent technology won the 1991 product of the year award from Electronic Design magazine.⁶³⁰ While SanDisk argues that the Toshiba example shows a failure of others, *i.e.* that Toshiba did not discover the benefits of permanent inhibit until 1994, ST counters that Toshiba discovered the benefits by 1990, as evidenced by Toshiba's own patent directed toward permanent inhibit (U.S. Patent No. 5,657,270).⁶³¹

Staff asserts that the analysis with respect to the issue of secondary considerations of non-obviousness for the '517 patent is basically the same as with respect to the '338 patent except that there has been a greater showing of commercial success, since SanDisk's NAND products practice the claimed invention, and there has been less showing of licensing, [

] ⁶³² Specifically, Staff asserts that none of the secondary considerations are clearly linked to the claimed invention. First, there has been no showing of a long-felt need coupled with a failure of others, [

] ⁶³³ Second, it is SanDisk's products in general,

⁶²⁹ RIB 80 citing *Ecolochem, Inc. v. Southern California Edison Co.*, 227 F.3d 1361, 1379 (Fed. Cir. 2000) ("*Ecolochem*") (simultaneous invention directly tied to level of knowledge attributable to one of ordinary skill in the art).

⁶³⁰ RIB 80 citing RX-1378 (ISSCC paper); RX-1370 (Simko CV) at ST560-H 45924.

⁶³¹ RIB 80 citing RX-1402 (Ohuchi continuation file wrapper) at ST560 519088.

⁶³² SIB 82.

⁶³³ SRB 39 citing SFF 357-59.

not the claimed invention, that have gained industry recognition and awards.⁶³⁴ Third, although SanDisk's NAND products have been a commercial success, it does not inherently mean that there is a nexus to the claimed invention, especially when there is a strong showing of obviousness.⁶³⁵ Therefore, Staff asserts that SanDisk's weak showing of secondary considerations does not rebut ST's showing of obviousness.⁶³⁶

SanDisk counters ST's arguments regarding simultaneity of invention. According to SanDisk, simultaneity of invention does not occur when a single element is known in the prior art, but when several near-contemporaneous references disclose the entire invention. In addition, SanDisk asserts that permanent inhibition is not the invention of the '517 patent.⁶³⁷

The undersigned agrees with ST and Staff that SanDisk has failed to rebut ST's strong showing of obviousness. While there is no doubt that SanDisk's NAND flash memory products have been a "success," both commercially and via industry awards and accolades, SanDisk has not shown any nexus between that success as attributable to what is claimed invention in the '517 patent. In addition, SanDisk has not shown a long-felt need coupled with a failure by others [

]⁶³⁸ Accordingly,

the undersigned finds that SanDisk has failed to rebut ST's showing of obviousness of the '517

⁶³⁴ SRB 39 citing CFF 6846, 6848, 6851, 6853, 6855.

⁶³⁵ SRB 39 citing *Dystar Textilfarben GmbH v. C.H. Patrick Co.*, 464 F.3d 1356, 1371-72 (Fed. Cir. 2006) ("*Dystar*").

⁶³⁶ SIB 82; SRB 39 citing *Dystar*, 464 F.3d at 1371-72 (finding that evidence of secondary considerations, including "considerable" commercial success, were insufficient to overcome the evidence that the claim was obvious); *Sibia*, 225 F.3d at 1358 (holding that a weak showing of secondary considerations does not outweigh a clear showing of obviousness).

⁶³⁷ CRB 38-39 citing *Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc.*, 796 F.2d 443, 449 (Fed. Cir. 1986) ("*Bausch & Lomb*").

⁶³⁸ Harari, Tr. at 354-55; RX-1802C (Pashley Witness Statement), at 235-36; CX-319/RX-712 (the '179 patent); RX-800 (JP100); RX-875 (GB '145).

patent.

4. Lack of Enablement/Inadequate Written Description/Best Mode

Based on the undersigned's above findings and conclusion that all of the asserted claims of the '517 patent are invalid as anticipated by the GB '145 reference and obvious based on the JP100 reference, in combination with the '179 patent and/or the '344 patent, the undersigned finds that it is not necessary to reach the issue of whether the '517 is invalid for lack of enablement, inadequate written description, or best mode as well.

E. Unenforceability

Based on the undersigned's above findings and conclusion that all of the asserted claims of the '517 patent are invalid as anticipated by the GB '145 reference and obvious based on the JP100 reference, in combination with the '179 patent and/or the '344 patent, the undersigned finds that it is not necessary to reach the issue of whether the '517 is unenforceable as well.

CONCLUSIONS OF LAW

1. The Commission has subject matter jurisdiction in this investigation.
2. The Commission has personal jurisdiction over ST.
3. ST's accused NAND products infringe claims 1, 3, 5, 6, 7, 8, and 10 of U.S. Patent No. 5,991,517 in violation of 35 U.S.C. § 271(a). In addition, all of ST's accused NAND products indirectly infringe these claims.
4. ST's accused NAND products do not infringe claims 12, 13, and 14 of U.S. Patent No. 5,991,517 in violation of 35 U.S.C. § 271(a).
5. ST's accused NOR products do not infringe claims 1, 3, 5, 6, 7, 8, 10, 12, 13, and 14 of U.S. Patent No. 5,991,517 in violation of 35 U.S.C. § 271(a).
6. An industry in the United States exists with respect to SanDisk's products that is protected by claim 1, 3, 5, 6, 7, 8, 10, and 12 of U.S. Patent No. 5,991,517, as required by 19 U.S.C. § 1337(a)(2) and (3).
7. An industry in the United States does not exist with respect to SanDisk's products that is protected by any claim of U.S. Patent No. 5,172,338, as required by 19 U.S.C. § 1337(a)(2) and (3).
8. Claims 1, 6, and 10 of U.S. Patent No. 5,991,517 are invalid under 35 U.S.C. § 102 for anticipation based on the GB '145 prior art reference.
9. Claims 1, 3, 5, 6, 10, 12, 13, and 14 of U.S. Patent No. 5,991,517 are not invalid under 35 U.S.C. § 102 for anticipation based the '179 patent.
10. Claims 1, 6, and 10 of U.S. Patent No. 5,991,517 are not invalid under 35 U.S.C. § 102 for anticipation based the M293 prior art reference.

11. Claims 1, 3, 5, 6, 7, 8, 10, 12, 13, and 14 of U.S. Patent No. 5,991,517 are invalid under 35 U.S.C. § 103 for obviousness based on JP100 by itself, or in combination with the '179 patent and/or the '344 patent.
12. Claims 1, 6, 7, 8, 10, 12, 13, and 14 of U.S. Patent No. 5,991,517 are not invalid under 35 U.S.C. § 103 for obviousness based on JP100 in combination with the '871 patent and/or the '541 patent.

INITIAL DETERMINATION

Based on the foregoing opinion, findings of fact, conclusions of law, the evidence, and the record as a whole, and having considered all pleadings and arguments, including the proposed findings of fact and conclusions of law, it is the Administrative Law Judge's Initial Determination that a violation of Section 337 of the Tariff Act of 1930, as amended, has not been found in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain NOR and NAND flash memory devices and products containing same, in connection with claims 1, 3, 5, 6, 7, 8, 10, 12, 13, and 14 of U.S. Patent No. 5,991,517 and has not been found in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain NOR and NAND flash memory devices and products containing same, in connection with claims 8, 9, 11, 27, 28, 32, 50, 51, and 64 of U.S. Patent No. 5,172,338. Furthermore, the Administrative Law Judge hereby determines that a domestic industry in the United States exists that practices U.S. Patent No. 5,991,517 and does not exist that practices U.S. Patent No. 5,172,338.

The Administrative Law Judge hereby CERTIFIES to the Commission this Initial Determination, together with the record of the hearing in this investigation consisting of the following: the transcript of the evidentiary hearing, with appropriate corrections as may hereafter be ordered by the Administrative Law Judge; and further the exhibits accepted into evidence in this investigation as listed in the attached exhibit lists.

Pursuant to 19 C.F.R. § 210.42(h), this Initial Determination shall become the determination of the Commission unless a party files a petition for review pursuant to 19 C.F.R. § 210.43(a) or the Commission, pursuant to 19 C.F.R. § 210.44, orders on its own motion a review of the Initial

Determination or certain issues therein.

RECOMMENDED DETERMINATION ON REMEDY AND BOND

Pursuant to Commission Rules 210.36(a) and 210.42(a)(1)(ii), the Administrative Law Judge is to consider evidence and argument on the issues of remedy and bonding and issue a recommended determination thereon.

VI. Remedy and Bonding

A. Limited Exclusion Order

Under Section 337(d), the Commission may issue either a limited or a general exclusion order. A limited exclusion order instructs the U.S. Customs Service to exclude from entry all articles that are covered by the patent at issue and that originate from a named respondent in the investigation. A general exclusion order instructs the U.S. Customs Service to exclude from entry all articles that are covered by the patent at issue, without regard to source. SanDisk requests that a limited exclusion order be issued that prohibits the importation of all infringing ST chips, as well as all downstream products which incorporate those chips, including memory cards, USB drives, and cell phones.⁶³⁹ SanDisk further argues that because the accused chips are produced abroad by ST's contractors, the exclusion order should extend to all accused chips manufactured and imported by or on behalf of ST in order to prevent evasion. According to SanDisk, such an order should include those accused chips manufactured and imported by its affiliated companies, parents, subsidiaries, licensees, contractors, joint venturers and other related business entities, and their successors or assigns.⁶⁴⁰

ST asserts that SanDisk's expert, Mr. Napper, only analyzed three categories of downstream

⁶³⁹ CIB 94-95.

⁶⁴⁰ CIB 95.

products—removable memory cards, USB drives, and cell phones—and that any request by SanDisk to exclude other types of downstream products should be rejected.⁶⁴¹

Staff asserts that the Commission should not issue an exclusion order that covers all downstream products, because the range of products that contain or could potentially contain a flash memory chip is enormous, which would place an undue burden on Customs that would disrupt legitimate trade.⁶⁴² Staff also asserts that the exclusion order should not extend to cell phones or DSL residential gateways.⁶⁴³ Staff does, however, agree that the Commission should issue an exclusion order that covers downstream products such as flash cards and USB drives.⁶⁴⁴

B. Downstream Products

Under Section 337, the Commission has broad discretion in selecting the form, scope, and extent of the remedy in a Section 337 proceeding. If the Commission finds a violation of Section 337, the Commission may issue an exclusion order that not only covers the articles found to infringe, but also covers “downstream products,” which are products that incorporate the infringing articles as components. The Commission has identified relevant factors to be considered in deciding whether to include downstream products in an exclusion order, commonly referred to as the *EPROMs* factors, including: (1) the value of the infringing articles compared to the value of the downstream products in which they are incorporated; (2) the identity of the manufacturer of the downstream products, i.e., whether it can be determined that the downstream products are manufactured by the respondent or by a third party; (3) the incremental value to the complainant of

⁶⁴¹ RIB 95.

⁶⁴² SIB 95.

⁶⁴³ SIB 95.

⁶⁴⁴ SIB 96-98.

the exclusion of downstream products; (4) the incremental detriment to respondents of exclusion of such products; (5) the burdens imposed on third parties resulting from exclusion of downstream products; (6) the availability of alternative downstream products that do not contain the infringing articles; (7) the likelihood that the downstream products actually contain the infringing articles and are thereby subject to exclusion; (8) the opportunity for evasion of an exclusion order that does not include downstream products; (9) the enforceability of an order by Customs; and any other factors the Commission determines to be relevant.⁶⁴⁵ In deciding whether to exclude downstream products, the Commission balances all of the above factors and nothing in the case law puts the burden of proof on any particular party with respect to the *EPROMs* factors.

SanDisk requests that the exclusion order not only cover the allegedly infringing chips that are found to infringe, but also cover all “downstream products” that incorporate the infringing chips as components. Examples of the types of “downstream products” that SanDisk wishes to exclude are memory cards, USB drives, cell phones, and DSL residential gateways. SanDisk contends that in order to have complete and effective relief, any limited exclusion order must include downstream products. SanDisk concludes that the *EPROMs* factors weigh in favor of an exclusion order.⁶⁴⁶ ST asserts that the exclusion order should not extend to any downstream products,⁶⁴⁷ while Staff asserts that the exclusion order should only extend to downstream products such as flash cards and USB drives.⁶⁴⁸

⁶⁴⁵ See *Certain Erasable Programmable Read-Only Memories*, Inv. No. 337-TA-276, USITC Pub. 2196, Comm’n Op. at 124-126, 136 (May 1989) (“*Certain EPROMs*”) *aff’d sub nom. Hyundai Elec. Indus. Co. v. U.S. Int’l Trade Comm’n*, 899 F.2d 1024 (Fed. Cir. 1990) (“*Hyundai*”).

⁶⁴⁶ CIB 94-98.

⁶⁴⁷ RIB 95.

⁶⁴⁸ SIB 96-98.

1. Factor 1: The value of the infringing articles compared to the value of the downstream products in which they are incorporated

SanDisk asserts that, with respect to factor 1, the value of the infringing ST flash chips is high compared to the value of the downstream products in which they are incorporated, both qualitatively and quantitatively. For example, SanDisk asserts that infringing ST chips enable the very function of memory cards, namely data transfer and storage, as well as the enhanced features driving demand for the newest and most advanced cell phones.⁶⁴⁹

ST asserts that, according to the evidence from third-party cell phone makers, flash chips only represent a small fraction of the value of the phones in which they are used, *i.e.* between 4.3-5.6%. ST also asserts that the flash chips only provide a small fraction of the overall functionality of the cell phone, the essential feature being to make telephone calls.⁶⁵⁰

Staff asserts that the first factor weighs in favor of an exclusion order covering downstream products because memory is an essential component in a flash card and USB drive, and that the memory constitutes a high proportion of the final cost of the device.⁶⁵¹

The undersigned agrees with SanDisk and Staff that the first *EPROMs* factor weighs in favor of including downstream products such as flash cards and USB drives in the exclusion order, on both a qualitative and quantitative basis because the evidence shows that flash memory is an essential component in a flash card and USB drive, and also constitute a high portion of the flash card and USB drive cost. The undersigned agrees with ST and Staff, however, that the first *EPROMs* factor weighs against including downstream products such as cellular telephones and DSL residential

⁶⁴⁹ CIB 96.

⁶⁵⁰ RIB 95.

⁶⁵¹ SIB 96 citing CX-2234C (Napper Direct) at 65-66.

gateways, because the flash memory only provides a small fraction of the overall functionality of these devices. Accordingly, the first *EPROMs* factor weighs in favor of including downstream products such as flash cards and USB drives in the exclusion order.

2. Factor 2: The identity of the manufacturer of the downstream products (i.e., are the downstream products manufactured by the party found to have committed the unfair act, or by third parties)

SanDisk asserts that, with respect to factor 2, the identify of many downstream product manufacturers has been confirmed during the investigation. SanDisk asserts that the following manufacturers incorporate infringing ST chips into their products and then import those products into the United States: []⁶⁵²

ST asserts that, except for very limited sales of memory cards, ST does not manufacture any of the downstream products and that the exclusion order would primarily affect third parties, who SanDisk chose not to name as respondents.⁶⁵³

Staff asserts that the second factor weighs in favor of an exclusion order covering downstream products because ST makes flash cards and works with certain customers to make USB drives.⁶⁵⁴

The undersigned agrees ST that the second *EPROMs* factor weighs against including downstream products in the exclusion because SanDisk, knowing the identity of the manufacturers and customers that incorporate ST's chips into their products, chose not to name these third parties

⁶⁵² CIB 96-97.

⁶⁵³ RIB 95-96.

⁶⁵⁴ SIB 96 citing Casagrande, Tr. 1510-11; CX-383C (NAND Flash presentation) at 115776-81; CX-486C (ST NAND Flash & Storage Media business plan) at 36355.

as respondents.⁶⁵⁵ Accordingly, the second *EPROMs* factor weighs against including downstream products such as flash cards and USB drives in the exclusion order.

3. Factor 3: The incremental value to the complainant for excluding the downstream products

SanDisk asserts that, with respect to factor 3, only an exclusion order which covers downstream products will provide full and effective relief in this investigation. According to SanDisk, flash memory chips cannot function without first being installed into a downstream products. SanDisk acknowledges that some infringing chips are imported into the U.S. separately, but that the vast majority of infringing ST chips enter the United States incorporated in downstream products.⁶⁵⁶

ST asserts that an exclusion order that only covers ST's flash memory chips and flash memory cards would provide effective and adequate relief to SanDisk. According to ST, from January to June 2006, ST sold[] units of the accused chips in the U.S., which is valued at []⁶⁵⁷ ST argues that there is little evidence that a significant quantity of downstream products containing ST's accused chips are actually imported into the U.S. because SanDisk did not quantify the volume of such imports.⁶⁵⁸ According to ST, its worldwide market share is relatively small. For example, ST's worldwide market share in NAND is []⁶⁵⁹ For NOR, ST's

⁶⁵⁵ See *Certain Baseband Processor Chips and Chipsets, Transmitter and Receiver (Radio) Chips, Power Control Chips, and Products Containing Same, Including Cellular Telephone Handsets*, Inv. No. 337-TA-543, Initial Determination at 275-76 (October 10, 2006) ("*Certain Baseband Processor Chips*").

⁶⁵⁶ CIB 97.

⁶⁵⁷ RIB 96 citing RX-1763C (ST flash chips North America 2006); RX-1800C (Mulhern Direct) at Q. 82, p. 15.

⁶⁵⁸ RIB 96.

⁶⁵⁹ RIB 96 citing RX-1738 (iSuppli Corp. Table "Q2 NAND market share"); RX-1800C
(continued...)

worldwide market share is [] however, ST asserts that only a fraction of those sales are for MLC NOR chips, which SanDisk accuses in this investigation.⁶⁶⁰ Furthermore, ST asserts that if third-parties were forced to find an alternative flash memory supplier, SanDisk would reap no benefit because SanDisk does not supply chips to manufacturers and does not produce or sell NOR flash chips at all; therefore, SanDisk would not make any additional sales (or receive any additional licensing revenue) if the exclusion order covered downstream products.⁶⁶¹

Staff asserts that the third factor weighs in favor of an exclusion order covering downstream products because SanDisk would benefit from an exclusion order covering flash cards and USB drives because SanDisk itself makes directly competitive products.⁶⁶²

The undersigned finds that the third *EPROMs* factor weighs in favor of including downstream products such as flash cards and USB drives in the exclusion because without an exclusion order covering flash cards and USB drives, SanDisk will be deprived from receiving full and effective relief in this investigation. Accordingly, the third *EPROMs* factor weighs in favor of including downstream products such as flash cards and USB drives in the exclusion order.

4. Factor 4: The incremental detriment to respondents if the products are excluded

SanDisk asserts that, with respect to factor 4, there is no evidence that ST would suffer undue harm if the Commission's order excludes downstream products containing the infringing chips. According to SanDisk, ST is a large, diversified company with a broad product line and that ST's

⁶⁵⁹(...continued)

(Mulhern Direct) at Q. 92, p. 17.

⁶⁶⁰ RIB 96 citing RX-1739 (iSuppli Corp. Table "NOR flash rankings"); RX-1800C (Mulhern Direct) at Q. 92, p. 17.

⁶⁶¹ RIB 96.

⁶⁶² SIB 96 citing Harari, Tr. 285-86; CX-2234C (Napper Direct) at 70.

NAND and MLC NOR sales constitute a relatively small proportion of its business. SanDisk contrasts this with its own business, the core of which consists of flash memory products. Furthermore, SanDisk asserts that there is no evidence that downstream ST customers would halt purchases of ST's flash memory chips, rather than simply aggregate products that contain the infringing chips, if a downstream exclusion order were to issue.⁶⁶³

ST asserts that an exclusion order covering downstream products would harm ST because an ST customer, being faced with the possibility of an exclusion order in the U.S., may go to other suppliers not only for the U.S. market, but for all markets. For example, ST asserts that [

] in order to comply with the exclusion order, and that [

] if such were the case.⁶⁶⁴

Staff asserts that the fourth factor weighs against an exclusion order covering downstream products because ST will suffer some detriment, but that it would be relatively small compared to the benefit to SanDisk.⁶⁶⁵

The undersigned agrees with ST and Staff that the fourth *EPROMs* factor weighs against including downstream products in the exclusion because of the incremental detriment to ST, including decreased sales and possible loss of customer base to ST. Accordingly, the fourth *EPROMs* factor weighs against including downstream products in the exclusion order.

⁶⁶³ CIB 97.

⁶⁶⁴ RIB 97.

⁶⁶⁵ SIB 97 citing CX-2234C (Napper Direct) at 72.

5. Factor 5: The burden borne by third parties as a result of excluding downstream products

SanDisk asserts that, with respect to factor 5, any burdens imposed on third parties due to the exclusion of downstream products would be minimal because the third parties could simply substitute the accused chips with chips manufactured by others.⁶⁶⁶

ST asserts that third party manufacturers, as well as exporters and distributors, would incur additional costs to identify and segregate products that have already been manufactured with ST chips, which weighs against the issuance of an exclusion order covering downstream products.⁶⁶⁷

Staff asserts that the fifth factor weighs against an exclusion order covering downstream products because there will be a burden on third parties, although Staff finds that such burden would be limited due to the natures of the products covered.⁶⁶⁸

The undersigned agrees with ST and Staff that the fifth *EPROMs* factor weighs against including downstream products in the exclusion because of the financial burden born by third parties, such as identifying and reconfiguring products if another chip manufacturer is used. Accordingly, the fifth *EPROMs* factor weighs against including downstream products in the exclusion order.

6. Factor 6: The availability of alternative downstream products that do not contain the infringing articles

SanDisk asserts that, with respect to factor 6, numerous downstream products that do not contain ST's infringing chips are available.⁶⁶⁹ ST does not address the sixth factor. Staff asserts that the sixth factor weighs in favor of an exclusion order covering downstream products because there

⁶⁶⁶ CIB 97.

⁶⁶⁷ RIB 97.

⁶⁶⁸ SIB 97.

⁶⁶⁹ CIB 97.

are many chips and downstream products that could replace ST's excluded products.⁶⁷⁰

The undersigned agrees with SanDisk and Staff that the sixth *EPROMs* factor weighs in favor of including downstream products such as flash cards and USB drives in the exclusion because there is a lot of competition in the flash memory chip industry with many alternative component suppliers available. Accordingly, the sixth *EPROMs* factor weighs in favor of including downstream products such as flash cards and USB drives in the exclusion order.

7. Factor 7: The likelihood that the downstream products actually contain the infringing article and, thus, are subject to the exclusion order

SanDisk asserts that, with respect to factor 7, ST and its customers sell and import into the United States, downstream products that contain infringing ST flash memory chips. According to SanDisk the number of imports is increasing rapidly and will likely continue in the future.⁶⁷¹

ST asserts that it only supplies [] of the world's NAND market, while supplying [] of the world's NOR market. According to ST, a large portion of the NOR market, however, includes chips that have not been accused in this investigation. Therefore, ST asserts that the likelihood that a downstream product will contain the accused chip is small and the exclusion order should not extend to downstream products.⁶⁷²

Staff asserts that the seventh factor weighs in favor of an exclusion order covering downstream products because there is evidence of downstream products, such as flash memory cards and USB drives, that incorporate the accused chips.⁶⁷³

The undersigned agrees with SanDisk and Staff that the seventh *EPROMs* factor weighs in

⁶⁷⁰ SIB 96 citing CX-2234C (Napper Direct) at 72-74.

⁶⁷¹ CIB 97-98.

⁶⁷² RIB 98.

⁶⁷³ SIB 96 citing CX-2234C (Napper Direct) at 74-75; []

favor of including downstream products such as flash cards and USB drives in the exclusion because ST has a clear market share in both NAND and NOR products. Accordingly, the seventh *EPROMs* factor weighs in favor of including downstream products such as flash cards and USB drives in the exclusion order.

8. Factor 8: The opportunity for evasion of an exclusion order

SanDisk asserts that, with respect to factor 8, ST could easily evade an exclusion order that does not prohibit the importation of downstream products simply by further directing its sales energies to customers who make their downstream products abroad.⁶⁷⁴

ST asserts that it sells a significant quantity of its flash memory chips to U.S. customers, including ST's three distributors. According to ST, these distributors have alternative chip suppliers and would have no incentive to attempt to evade an exclusion order by purchasing end products in lieu of flash memory chips.⁶⁷⁵

Staff asserts that the eighth factor weighs in favor of an exclusion order covering downstream products because there is an opportunity for evasion of the order because the majority of ST's sales are made abroad to companies that incorporate the chips into downstream products.⁶⁷⁶

The undersigned agrees with SanDisk and Staff that the eighth *EPROMs* factor weighs in favor of including downstream products such as flash cards and USB drives in the exclusion because without an exclusion order covering flash cards and USB drives, there is an opportunity for customers to incorporate the accused infringing chips into downstream products. Accordingly, the eighth *EPROMs* factor weighs in favor of including downstream products such as flash cards and

⁶⁷⁴ CIB 98.

⁶⁷⁵ RIB 98.

⁶⁷⁶ SIB 97 citing CX-2234C (Napper Direct) at 76-78; CX-2296C (Napper Rebuttal) at 25.

The title company's request for relief is supported by Rafkind v. Chase Manhattan Bank, 1992 WL 380291 (S.D.N.Y. 1992). In Rafkind, the Court summarized the applicable law as follows:

"A judgment debtor may contract with a third party to withhold funds to which the judgment debtor would otherwise be entitled, for purpose of paying certain of the judgment debtor's creditors. See M.F. Hickey, 258 N.Y.S.2d at 130 (1st Dept. 1965). Once the judgment debtor has contracted away his rights to funds to pay certain creditors, his interest in the funds is limited to the funds remaining after such creditors are paid. Id. (citing United States Fidelity & Guaranty Co. v. Triborough Bridge Auth., 297 N.Y. 31, 37, 74 N.E.2d 226 (1947)). Any subsequent judgment creditor has only a contingent interest in the funds that vests only if there is a surplus after paying the other creditors. See M.F. Hickey, 258 N.Y.S.2d at 130; see also U.R.C. Inc. v. Applied Images, Inc., 106 Misc.2d 1034, 1040, 431 N.Y.S.2d 859, 862 (Sup. Ct. 1980) (citing M.F. Hickey); United States v. Sterling Nat'l Bank and Trust Co., 494 F.2d 919, 922 (2d Cir. 1974) (citing United States v. Hampton Garment Co., 71-1 U.S. Tax Case 9357 (S.D.N.Y. 1971))."

In so holding, the Rafkind court relied in part upon M.F. Hickey, v. Port of New York Authority, 258 N.Y.S. 2d 129 (1st Dept. 1965), where the Appellate Division, First Department, found that a contractor had an "interest, albeit a contingent one, in the withheld fund, and this interest will vest if any surplus remains after the payment of all just claims. . . . Consequently, the judgment creditor was entitled to a declaration that it will be entitled to recover any such surplus as may remain." Id. At 130.

Other cases also support the relief requested in the special proceeding. For example, U.R.C. Inc. v. Applied Images, Inc., 431 N.Y.S.2d 859 (Sup. Ct. Nassau Co. 1980) has been widely followed in New York State. Distilled to its legal significance, U.R.C. holds that traditional escrow or collateral deposits should be considered exempt from execution, except for any "excess" over the balance due to the party which established the escrow fund for security purposes